# Pulse Control LSI for Serial Bus Control

# PCD2112A

# User's manual

Impress, not just satisfy
Nippon Pulse Motor Co., Ltd.

# [Preface]

Thank you for choosing “PCD2112A” pulse controlled LSI.

Please read this manual thoroughly to become familiar with PCD2112A before using it.

Please note that the “Handling Precautions” concerning the mounting of this product are explained at the end of this manual.

# [Precautions for indications]

1) Reproduction of this manual, in whole or in part, is prohibited by the Copyright Act.
2) The contents of this manual are subject to change without prior notice in accordance with performance and quality improvement.
3) The contents of this manual are intended to be thorough, but should you find any uncertain subject, errors, or missing information, please feel free to contact us.
4) Regardless of the abovementioned items, we are not liable for any damages caused by the use of this product.

# [Description]

1) Negative logic terminal names and negative logic signal names are not decorated with overbar nor “#”.
   For the logics, see “3.3 Terminal functions”.
2) “0” in bit description of registers etc. indicates the bit position and that only “0” can be written and only “0” can be read out.
3) The specific bit of a register is shown as “register name. bit name”; (e.g. RMD.MSDE)
4) In the description of operating speed, when the subject is applied for both “FH1” and “FH2”, they are collectively referred to as “FH”. In the explanation of registers for speed, “RFH1” and “RFH2” speed registers are also collectively referred to as “RFH”. In the explanation of commands, “STAFH1” and “STAFH2” are also collectively referred to as “STAFH”.
5) In the description of end limit terminals, when the subjects are common to both “PEL terminal” and “MEL terminal”, they are collectively referred to as “EL terminals”.
   In the description of end limit signals, when they are common both to “PEL signal” and “MEL signal”, they are also collectively referred to as “EL signals”.
6) If the time is indicated, the value of “Reference clock frequency = 9.8304 MHz” is indicated unless otherwise specified.
7) There are “ON” and “OFF” in the signal status. In the case of positive logic, “H level” or “1” is “ON” state. In the case of negative logic, “L level” or “0” is “ON” state.
8) The value suffix “b” represents a binary number, and “h” represents a hexadecimal number. Suffixes are not added to decimal numbers.
   Suffixes may not be added to binary and hexadecimal numbers for some figures, tables, or values that are the same as decimal numbers.

# INDEX

# 1. Outline and features

## 1.1 Outline

PCD2112A is a pulse generator LSI that can connect to CPU by 4-wire serial bus I/F.
Serial bus I/F do not require many signal lines, unlike the parallel bus I/F.
A smaller package CPU can be selected, and general-purpose ports of CPU can be used effectively.
In addition to “CPU-connected system” controlled by CPU, “stand-alone operation system” operating with external EEPROM, is built-in.

## 1.2 Features

◆ Serial bus I/F

Since 4-wire serial bus is used to connect with CPU, the number of occupied terminals for bus control in CPU can be reduced, so that the number of open general-purpose I/O terminals increase.
From CPU, you can access to PCD2112A in the same way as 4-wire serial EEPROM.

◆ Small package

The use of a serial bus has resulted in a compact package (TQFP-48) with multiple functions.
The external dimensions are 9 mm square, and the molded part is 7 mm square.

◆ 3.3 V single power supply

It operates with a single power supply of 3.3 V ± 0.3 V.
The output signal level is 3.3 V, but the input signal level can be 5 V (TTL).

◆ High-speed pulse train output

When the reference clock frequency is 9.8304 MHz (standard), 2.4 Mpps can be output.
When it is 20 MHz, with is the maximum frequency, up to 5 Mpps can be output.
Output pulse mode can be selected out of common-pulse (OUT and DIR), 2-pulses (positive and negative), and 90-degree phase difference 4x (= multiplication) (A-phase and B-phase).

◆ Excitation sequence signal output for 2-phase stepping motor

Two types of drive and two types of excitation can be used to output excitation sequence signals.

◆ Acceleration/deceleration control

Linear acceleration/deceleration and S-curve acceleration/deceleration can be performed.
For S-curve acceleration/deceleration, linear acceleration/deceleration sections can be inserted in the middle part (S-curve section setting). The acceleration and deceleration characteristics can be set independently (independent setting is not available when using slow-down point auto-setting function).

◆ Target speed override

Speed can be changed during operation.

◆ Triangle drive avoidance function (FH correction function)

When the total amount of feeding pulses is small, the maximum speed is automatically lowered to avoid triangular driving.
This function is available for operation mode of incremental movement in positioning control and switch control.

◆ Simultaneous start function

When multiple LSIs are used and if all STA terminals are connected, they can start at the same time.

◆Various operation modes

- Continuous movement (command control, manual pulser control, switch control )
- Origin return (stop at origin sensor, feeding amount limit stop)
- Escaping (Origin sensor, End limit sensor)
- Incremental movement (positioning control, manual pulser control, switch control).
- Timer

◆ Stand-alone operation system

If you connect a 4-wire serial EEPROM to PCD2112A, controls can be done without connecting to CPU.
Up to 32 types of operation patterns can be stored in EEPROM.

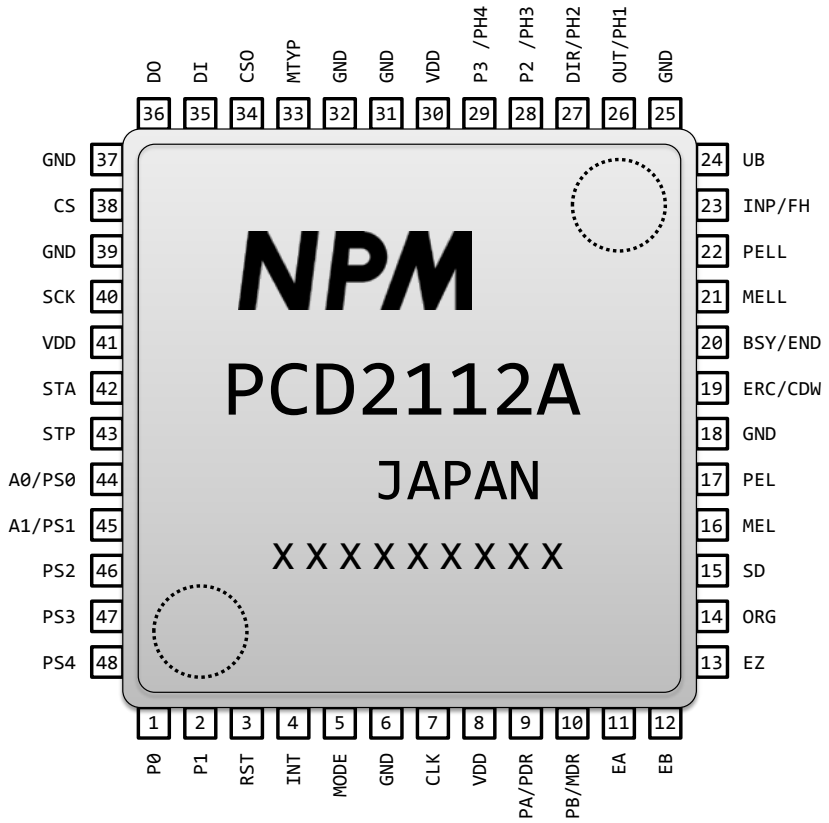
# 2. Specifications

## 2.1 Basic specifications

| Item | Description |
|---|---|
| Power supply | +3.3 V ± 0.3 V |
| Reference clock | Standard: 9.8304 MHz (20 MHz max.) |
| CPU I/F | 4-wire serial bus |
| Output pulse number (=feeding amount) setting range | 0 to 268,435,455 (28 bit) |
| Number of speed setting steps | 1 to 8,191 (13 bit) |
| Speed magnification setting range | 0.5 to 300x (reference clock 9.8304 MHz)<br>0.5 x: 0.5 to 4,095.5 pps<br>1 x: 1 to 8,191 pps<br>300 x: 300 to 2,457,300 pps |
| Number of speed setting register | 3 registers : FL, FH1, and FH2 |
| Slow-down point (=ramping down point) setting range | 0 to 16,777,215 (24 bit) |
| Characteristic of acceleration/deceleration | · Linear acceleration/deceleration<br>· S-curve acceleration/deceleration |
| Acceleration rate setting range | 1 to 65,535 (16 bit) |
| Deceleration rate setting range | 1 to 65,535 (16 bit) |
| Up/down counter | −2,147,483,648 to +2,147,483,647 (32 bit) |
| General-purpose I/O terminal | 4 bits (2 bits are output fixed, 2 bits are input/output selectable) |
| The excitation sequence output | Excitation sequence output for stepping motors<br>· Driving method: selection of unipolar drive or bipolar drive<br>· Excitation method: selection of full step or half step |
| Typical operation example | Continuous movement by command control<br>· Origin return movement by origin signal control<br>· Origin return with feeding amount limit setting by origin signal control<br>· Origin escape by origin signal control<br>· EL escape by EL signal control<br>· Incremental movement of positioning control<br>· Timer by positioning control<br>· Continuous movement and incremental movement by switch control<br>· Continuous movement and incremental movement by manual pulser control |
| Ambient temperature | −40 to + 85 ºC |
| Storage temperature | −65 to + 150 ºC |
| Package | 48 pin TQFP (7 x 7 mm: molded part) |
| Weight | 0.13 g |

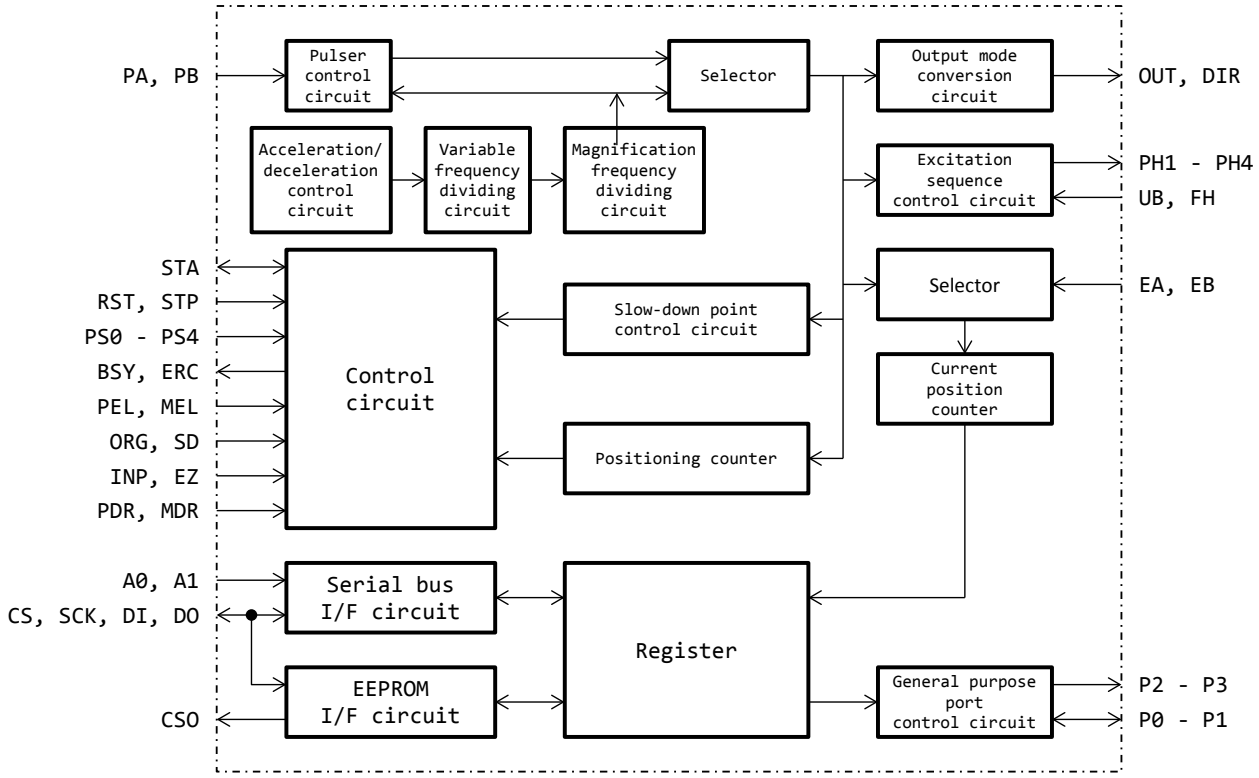
Note:
1) During operation, the target position cannot be changed, in other words, target position override is not available. (Speed can be changed.)
2) During slow-down point auto setting, be sure to set the acceleration and deceleration characteristics to be the same.

## 2.2 Terminal assignment diagram




Note: No. 1 pin is located at the bottom left with the type name making “1”.

## 2.3 Block diagram



# 2.4 Terminal list

U/D column (internal circuit) ..... PD: Pull-Down (40 kΩ to 240 kΩ) built-in resistor, OD: Open drain.
Process column (when not in use) ..... Open: unconnected,
(PD): connected to pull-down (5 kΩ to 10 kΩ) or no connection.
[PD]: Connected to pull-down (5 kΩ to 10 kΩ), no connection or connected to GND.
[GN]: Connect to GND.
TTL column (TTL I/F) ..... ○: 5 V (TTL) I/F is OK. (Output terminals do not reach 5 V even if they are pulled up externally).

| Pin | Name | I/O | U/D | Process | TTL | $I_{OH}$ | $I_{OL}$ | Description |
|---|---|---|---|---|---|---|---|---|
| 1 | P0 | I/O | PD | (PD) | ○ | −6 mA | 6 mA | General-purpose I/O terminal 0 |
| 2 | P1 | I/O | PD | (PD) | ○ | −6 mA | 6 mA | General-purpose I/O terminal 1 |
| 3 | RST | I | PD | - | ○ | - | - | Reset |
| 4 | INT | O | OD | Open | ○ | −6 mA | 6 mA | Interrupt request |
| 5 | MODE | I | PD | - | ○ | - | - | Operation mode (L: CPU-connected, H: Stand-alone) |
| 6 | GND | I | - | - | - | - | - | GND |
| 7 | CLK | I | - | - | ○ | - | - | Reference clock |
| 8 | VDD | I | - | - | - | - | - | +3.3 V |
| 9 | PA/PDR | I | PD | [PD] | ○ | - | - | Pulser A-phase / positive direction operation switch |
| 10 | PB/MDR | I | PD | [PD] | ○ | - | - | Pulser B-phase / negative direction operation switch |
| 11 | EA | I | PD | [PD] | ○ | - | - | Encoder A-phase |
| 12 | EB | I | PD | [PD] | ○ | - | - | Encoder B-phase |
| 13 | EZ | I | PD | [PD] | ○ | - | - | Encoder Z-phase |
| 14 | ORG | I | PD | [PD] | ○ | - | - | Origin sensor |
| 15 | SD | I | PD | [PD] | ○ | - | - | Deceleration sensor (common in ± moving direction) |
| 16 | MEL | I | PD | [PD] | ○ | - | - | Negative direction end limit |
| 17 | PEL | I | PD | [PD] | ○ | - | - | Positive direction end limit |
| 18 | GND | I | - | - | - | - | - | GND |
| 19 | ERC/CDW | O | - | Open | ○ | −12 mA | 12 mA | Deviation counter clear / current down |
| 20 | BSY/END | O | - | Open | ○ | −12 mA | 12 mA | In operation (busy) / operation complete |
| 21 | MELL | I | PD | [GN] | ○ | - | - | MEL signal input logic |
| 22 | PELL | I | PD | [GN] | ○ | - | - | PEL signal input logic |
| 23 | INP/FH | I | PD | [PD] | ○ | - | - | In-position / excitation mode: (L: Full step – H: Half step ) |
| 24 | UB | I | PD | [PD] | ○ | - | - | Drive mode: L: Unipolar, H: Bipolar |
| 25 | GND | I | - | - | - | - | - | GND |
| 26 | OUT/PH1 | O | - | Open | ○ | −12 mA | 12 mA | Pulse train signal / 1-phase excitation signal |
| 27 | DIR/PH2 | O | - | Open | ○ | −12 mA | 12 mA | Operation direction signal/ 2-phase excitation signal |
| 28 | P2/PH3 | O | PD | Open | ○ | −12 mA | 12 mA | General-purpose output terminal 2 / 3 phase excitation signal |
| 29 | P3/PH4 | O | PD | Open | ○ | −12 mA | 12 mA | General-purpose output terminal 3 / 4 phase excitation signal |
| 30 | VDD | I | - | - | - | - | - | +3.3 V |
| 31 | GND | I | - | - | - | - | - | Input terminal for shipping inspection (connect to GND) |
| 32 | GND | I | - | - | - | - | - | Input terminal for shipping inspection (connect to GND) |
| 33 | MTYP | I | PD | - | ○ | - | - | Operation pulse selection<br>(L: Pulse train output, H: excitation sequence output) |
| 34 | CSO | O | - | Open | ○ | −6 mA | 6 mA | CS (Chip select) output for EEPROM |
| 35 | DI | I/O | PD | - | ○ | −6 mA | 6 mA | For serial communication: data input<br>(output when MODE = H level) |
| 36 | DO | I/O | PD | - | ○ | −6 mA | 6 mA | For serial communication: data output<br>(input when MODE = H level) |
| 37 | GND | I | - | - | - | - | - | GND |
| 38 | CS | I/O | PD | Open | ○ | −6 mA | 6 mA | For serial communication: chip select input (outputs when MODE = H level) |
| 39 | GND | I | - | - | - | - | - | GND |
| 40 | SCK | I/O | PD | - | ○ | −6 mA | 6 mA | For serial communication: synchronous clock input (outputs when MODE = H level) |
| 41 | VDD | I | - | - | - | - | - | +3.3 V |
| 42 | STA | I/O | PD | Open | ○ | −6 mA | 6 mA | External start |
| 43 | STP | I | PD | [PD] | ○ | - | - | External stop |
| 44 | A0/PS0 | I | PD | [PD] | ○ | - | - | LSI selection 0 / pattern selection 0 |
| 45 | A1/PS1 | I | PD | [PD] | ○ | - | - | LSI selection 1 / pattern selection 1 |
| 46 | PS2 | I | PD | (PD) | ○ | - | - | Pattern selection 2 |
| 47 | PS3 | I | PD | (PD) | ○ | - | - | Pattern selection 3 |
| 48 | PS4 | I | PD | (PD) | ○ | - | - | Pattern selection 4 |

# 2.5 System modes

With PCD2112A, the following four types of systems can be selected by MODE terminal and MTYP terminal.
Do not change the settings while the power is ON. Some input terminals may change to output terminals if the settings are changed. Be careful when designing an external circuit.

1) CPU-connected pulse train output system (MODE = L, MTYP = L)
   4-wire serial bus is connected to CPU for control. Pulse train signals are output.

2) CPU-connected excitation sequence output system (MODE = L, MTYP = H)
   4-wire serial bus is connected to CPU for control. Excitation sequence signals are output.
   Excitation sequence can be selected from four types depending on UB terminal and FH terminal.

3) Stand-alone pulse train output system (MODE = H, MTYP = L)
   Reads the operation patterns specified by PS0 to PS4 terminals from an external EEPROM; up to 32 operation patterns have been written in the EEPROM.
   Pulse train signals are output according to the operation pattern.
   CPU is required to write patterns to EEPROM, but it is not required for operation.

4) Stand-alone excitation sequence output system (MODE = H, MTYP = H)
   Reads the operation patterns specified by PS0 to PS4 terminals from an external EEPROM; up to 32 operation patterns have been written in the EEPROM.
   Excitation sequence signals are output according to the operation pattern.
   CPU is required to write patterns to EEPROM, but is not required for operation.
   The excitation sequence can be selected from four types depending on UB terminal and FH terminal.

| System modes | | | | MODE | MTYP | UB | FH |
|---|---|---|---|---|---|---|---|
| CPU-connected operation | Pulse train output | | | L | L | L | (INP) |
| | Excitation sequence output | Unipolar | Full-step | L | H | L | L |
| | | | Half-step | L | H | L | H |
| | | Bipolar | Full-step | L | H | H | L |
| | | | Half-step | L | H | H | H |
| Stand-alone operation | Pulse train output | | | H | L | L | (INP) |
| | Excitation sequence output | Unipolar | Full-step | H | H | L | L |
| | | | Half-step | H | H | L | H |
| | | Bipolar | Full-step | H | H | H | L |
| | | | Half-step | H | H | H | H |

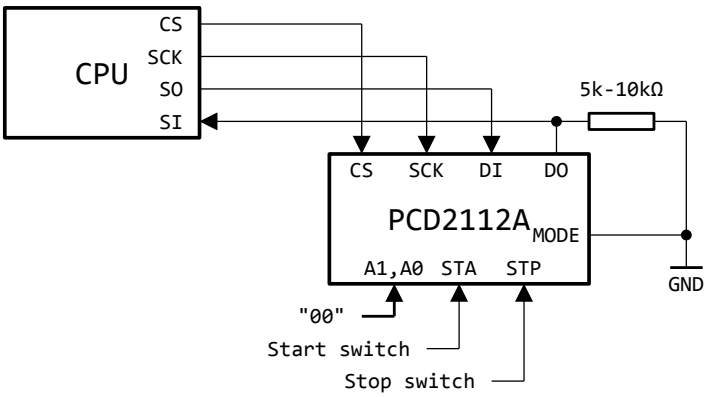
Note 1: In pulse train output mode, UB terminal is disabled.
UB terminal has a built-in pull-down resistor, so set to L-level to lower the current consumption.

Note 2: In pulse train output mode, INP/FH terminal become INP terminal.

## 2.5.1 CPU-connected system (MODE = L)

PCD2112A is connected to CPU by 4-wire serial I/F.
Multiple LSIs can be connected with one CS output.
To control products other than “PCD2112A”, prepare CS output separately.

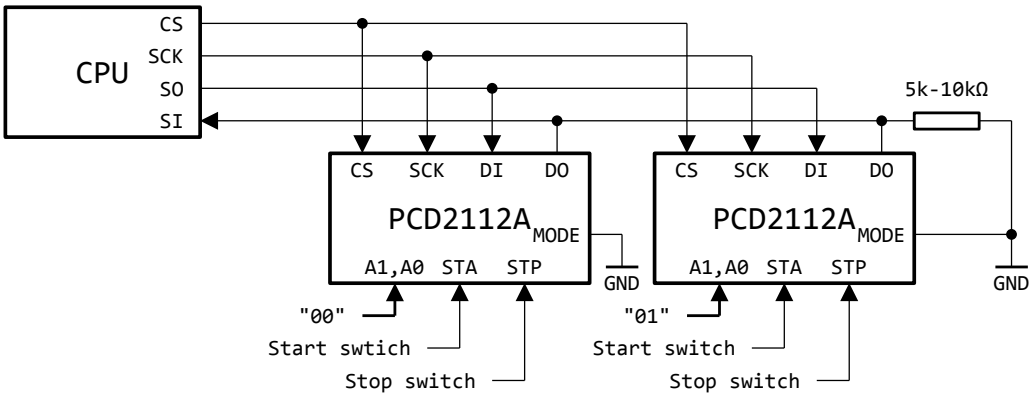
1) Normal connection




Both start and stop can be done from CPU.

Note: Connect a pull-down resistor for the purpose of preventing breakage of CPU and PCD2112A when floating.

2) Multiple connections




Both start and stop can be done from CPU.

Note: Connect a pull-down resistor to prevent CPU and PCD2112A from a breakage when floating.

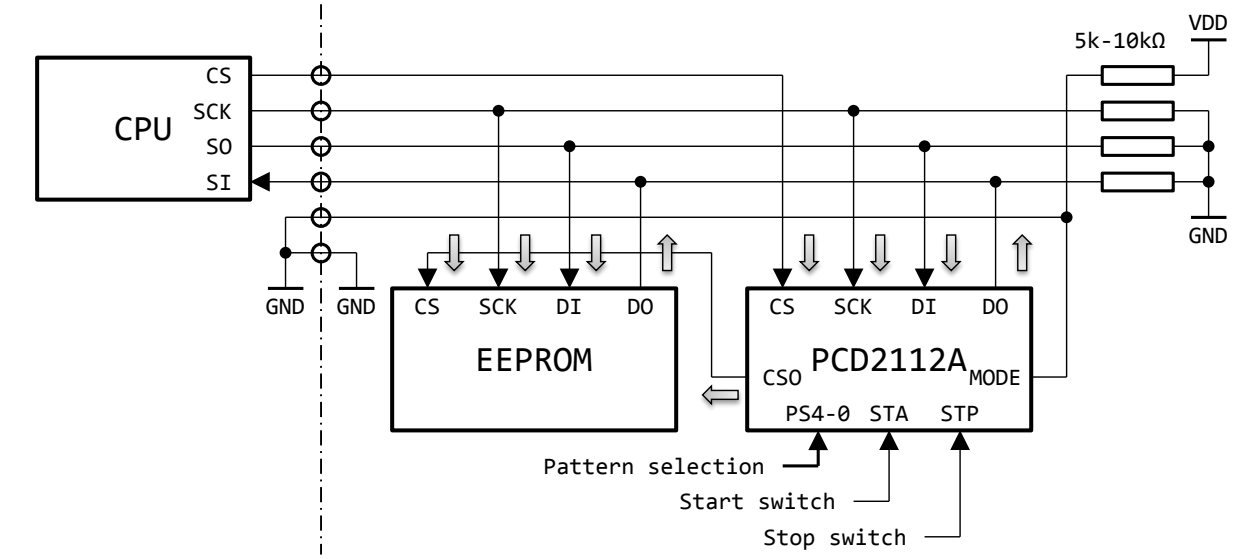
## 2.5.2 Stand-alone operation system (MODE = H)

An operation is selected by pattern selection terminals to perform. Up to 32 types of operation patterns have been stored in the 4-wire serial EEPROM. In the stand-alone operation system, this LSI and EEPROM are used in one configuration for one serial I/F. Writing to EEPROM is done by CPU-connected system.
In this case, CSO terminal of "PCD2112A" is connected to CS terminal of EEPROM, so do not connect CS terminal of CPU to CS terminal of EEPROM.

Note: External pull-down of SCK, DI, and DO terminals in the circuit diagram below can be done by pull-up. Pull-down can reduce the power consumption of the board.

1) Writing to EEPROM

Writing operation patterns to EEPROM is performed from CPU with separately prepared CPU.

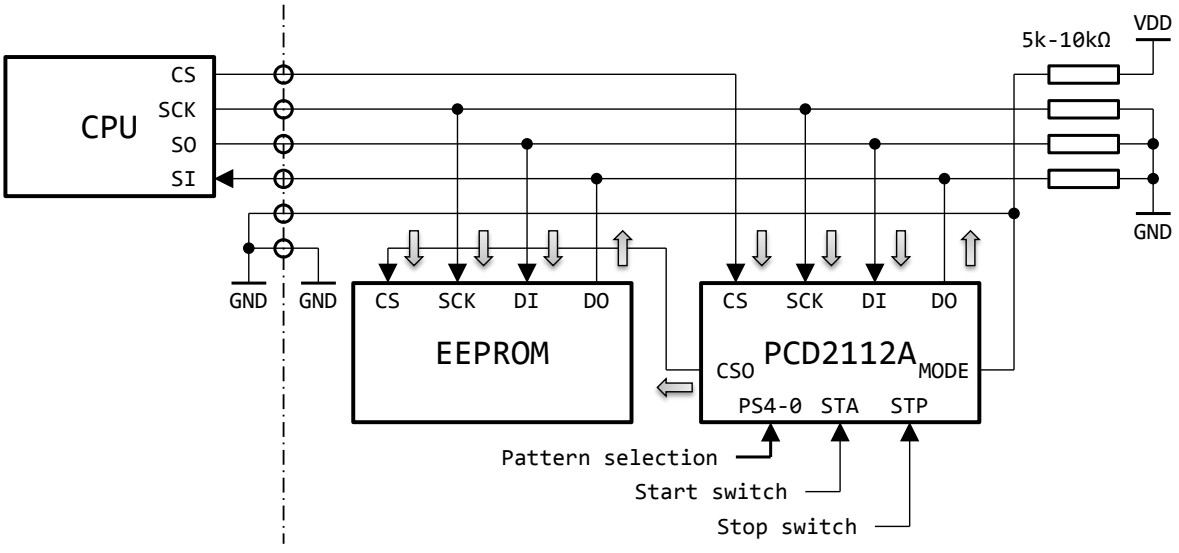



SCK (Serial clock) is output by CPU.
CS (Chip select) for PCD2112A is also output by CPU and CS for EEPROM is output via CSO of PCD2112A.
SO/SI (Serial data) is used in common between CPU and EEPROM, and also between CPU and PCD2112A.

Note: PS0 and PS1 terminals for pattern selection are A0 and A1 terminals for LSI selection respectively because they are used in CPU-connected system.
When communicating with CPU, match the set values of A0 and A1 terminals and bits 4 and 5 in bus control command.

2) When performing an stand-alone operation system

After writing operation patterns and stored them in an EEPROM, CPU can be disconnected before an operation.
In the circuit shown below, MODE signal becomes H level when CPU is disconnected.




SCK (Serial clock) and CS (Chip Select) are output by PCD2112A.
SO/SI (Serial data) is communicated between PCD2112A and EEPROM.

# 3. Terminal descriptions

## 3.1 Outline of terminal functions

| Terminal name | Terminal number | I/O | Logic setting | Description |
|---|---|---|---|---|
| Power supply input | | | | |
| VDD | 8, 30, 41 | I | - | +3.3 V |
| GND | 6, 18, 25, 31, 32, 37, 39 | I | - | GND |
| System selection | | | | |
| MODE | 5 | I | - | L: CPU-connected system<br>H: Stand-alone operation system |
| MTYP | 33 | I | - | L: Pulse train H: Excitation sequence |
| Serial communication (MODE = L-level: CPU-connected) | | | | |
| CS | 38 | I | - | For serial communication: chip select input |
| SCK | 40 | I | - | For serial communication:<br>Synchronous clock input |
| DI | 35 | I | - | For serial communication: data input |
| DO | 36 | O | - | For serial communication: data output |
| Serial communication (MODE = H-level: stand-alone operation ) | | | | |
| CS | 38 | O | - | Not used |
| SCK | 40 | O | - | For serial communication: synchronous clock output |
| DI | 35 | O | - | For serial communication: data output |
| DO | 36 | I | - | For serial communication: data input |
| For motion control | | | | |
| RST | 3 | I | - | Reset |
| CLK | 7 | I | - | Reference clock |
| A0, A1 | 44, 45 | I | - | LSI selection |
| INT | 4 | O | - | Interrupt request |
| BSY/END | 20 | O | - | Busy / Operation end |
| ERC/CDW | 19 | O | RENV1.ERCL | Deviation counter clear / Current down |
| INP | 23 | I | RENV1.INPL | In-position (positioning completes) |
| STA | 42 | I/O | - | External start |
| STP | 43 | I | RENV1.STPL | External stop |
| P0, P1 | 1, 2 | I/O | - | General-purpose I/O terminals 0 and 1 |
| P2, P3 | 28, 29 | O | - | General purpose output terminals 2 and 3 |
| For sensor input | | | | |
| PA, PB | 9, 10 | I | RENV2.PIM | Manual pulser |
| PDR, MDR | 9, 10 | I | RENV1.DRL | Drive switch |
| EA, EB | 11, 12 | I | RENV2.EIM | Encoder |
| EZ | 13 | I | RENV2.EZL | Encoder Z phase |
| PELL, MELL | 22, 21 | I | - | EL signal input logic |
| PEL, MEL | 17, 16 | I | PELL, MELL | End limit sensor |
| ORG | 14 | I | RENV1.ORGL | Origin sensor |
| SD | 15 | I | RENV1.SDL | Deceleration sensor |
| For motor drive | | | | |
| OUT, DIR | 26, 27 | O | RENV1.PMD | Output pulse |
| FH | 23 | I | - | L: Full step, H: Half step |
| UB | 24 | I | - | L: Unipolar drive, H: Bipolar drive |
| PH1, PH2, PH3, PH4 | 26, 27, 28, 29 | O | - | Excitation sequence |
| For stand-alone operation | | | | |
| CSO | 34 | O | - | Chip select for EEPROM |
| PS0, PS1, PS2, PS3, PS4 | 44, 45, 46, 47, 48 | I | - | Pattern selection; 0 to 4 |

Note: The above table classifies the functions, and some terminals have multiple functions (share the same terminal numbers).

# 3.2 Terminal functions in each system mode

Functions of the following terminals will be changed depending on the system mode.

| Mode / Terminal name | | CPU-connected system | | | | Stand-alone operation system | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Pulse train output | | Excitation sequence output | | Pulse train output | | Excitation sequence output | |
| | | Terminal function | I/O | Terminal function | I/O | Terminal function | I/O | Terminal function | I/O |
| 5 | MODE | (Low) | I | (Low) | I | (High) | I | (High) | I |
| 33 | MTYP | (Low) | I | (High) | I | (Low) | I | (High) | I |
| 40 | SCK | SCK | I | SCK | I | SCK | O | SCK | O |
| 35 | DI | DI | I | DI | I | DI | O | DI | O |
| 36 | DO | DO | O | DO | O | DO | I | DO | I |
| 38 | CS | CS | I | CS | I | (Same as CSO) | O | (Same as CSO) | O |
| 44 | A0/PS0 | A0 | I | A0 | I | PS0 | I | PS0 | I |
| 45 | A1/PS1 | A1 | I | A1 | I | PS1 | I | PS1 | I |
| 46 | PS2 | (*) | I | (*) | I | PS2 | I | PS2 | I |
| 47 | PS3 | (*) | I | (*) | I | PS3 | I | PS3 | I |
| 48 | PS4 | (*) | I | (*) | I | PS4 | I | PS4 | I |
| 1 | P0 | P0 | I/O | P0 | I/O | (*) | O | (*) | O |
| 2 | P1 | P1 | I/O | P1 | I/O | (*) | O | (*) | O |
| 24 | UB | (*) | I | UB | I | (*) | I | UB | I |
| 23 | INP/FH | INP | I | FH | I | INP | I | FH | I |
| 26 | OUT/PH1 | OUT | O | PH1 | O | OUT | O | PH1 | O |
| 27 | DIR/PH2 | DIR | O | PH2 | O | DIR | O | PH2 | O |
| 28 | P2/PH3 | P2 | O | PH3 | O | (*) | O | PH3 | O |
| 29 | P3/PH4 | P3 | O | PH4 | O | (*) | O | PH4 | O |

Note 1: For terminals with multiple names (=multiple functions), the name / function will be selected by “Environment setting register”.
Note 2: “(Low)” and “(High)” indicate the level to be set for input.
(*): Please pull down (with 5 kΩ to 10 kΩ).

# 3.3 Terminal functions

## 3.3.1 CLK [7]

Input terminal of reference clock. (Standard: 9.8304 MHz)
The accuracy of reference clock frequency affects the speed accuracy of output pulses.
It also affects start timing, input sensitivity of STA, ORG, MEL, PEL, and STP signals, and write/read timing.

## 3.3.2 RST [3]

Input terminal of reset signals.
Inputs 8 or more CLK signals while “RST = L”.
Then, you can use it after inputting 8 or more CLK signals while “RST = H”.
Be sure to reset at least once after turning ON the power and before starting an operation.
The status after the reset is shown in the table below:

| Item | Reset status (Default status) |
|---|---|
| Internal register | 0 |
| Control command | 0 |
| P0 ~ P1 terminal | Input terminal (*1) |
| OUT and DIR terminals | H level |
| INT terminal | H level |
| ERC/CDW terminal | H level |
| BSY/END terminal | H level |
| PH1, PH2, PH3 and PH4 terminal | STEP0 sequencing status (*2) |
| P2 and P3 terminals (MTYP terminal = L level) | L level |

*1 : It may be an output terminal between power ON and resetting.
*2 : See “10.6.2 PH1 to PH4 signals”.

## 3.3.3 MODE [5]

Input terminal for setting “System mode” of PCD2112A.
For information on “System mode”, see “2.5 System modes”.

| MODE | System mode |
|---|---|
| L | CPU-connected system |
| H | Stand-alone operation system (EEPROM connected) |

## 3.3.4 MTYP [33]

Input terminal for selecting the motor control method.

| MTYP | Mode | Description |
|---|---|---|
| L | Pulse train output mode | INP/FH terminal functions as INP inputs.<br>DIR/PH1 terminal outputs pulse trains.<br>DIR/PH2 terminal outputs direction signals.<br>P2/PH3 terminal functions as general-purpose output terminal P2.<br>P3/PH4 terminal functions as general-purpose output terminal P3. |
| H | Excitation-sequence output mode | INP/FH terminal functions as FH input.<br>OUT/PH1 to P3/PH4 terminals output excitation sequence signals. |

## 3.3.5 INT [4]

Output terminal for interrupt request (INT) signals to CPU.
Multiple LSIs can be wired-OR connected by using a pull-up resistor (5 kΩ to 10 kΩ) to the outside.
When an interrupt condition occurs, it becomes “L level”.
The interrupt conditions are set by bits 22 to 17 of RENV2 register.
You can mask the outputs with RENV2.MSKI bit.
INT signal can be output by stopping with EL, STP, or SD signal without setting the interrupt condition.

## 3.3.6 SCK [40], DI [35], DO [36], CS [38], CSO [34]

The following are the terminals for serial communication:

| Setting / Terminal name | MODE = L (CPU-connected system ) | MODE = H (Stand-alone operation system ) |
|---|---|---|
| SCK | Synchronous clock input of serial signal | Synchronous clock output of serial signal |
| DI | Serial input signal | Serial output signal |
| DO | Serial output signal | Serial input signal |
| CS | Chip select Input | The same signal as CSO is output. * |
| CSO | Chip select output to EEPROM (when both PCD2112A and EEPROM are controlled by CPU using one CS). * | |

* : They can be opened when they are not in use.

## 3.3.7 PA/PDR [9], PB/MDR [10]

Used when “RMD.MOD = 7h to Ah”.
It works as follows in accordance with RMD.MOD bit.

| Setting / Terminal name | RMD.MOD = 9h, Ah | RMD.MOD = 7h, 8h |
|---|---|---|
| PA/PDR | PA (manual pulser) | PDR (drive switch) |
| PB/MDR | PB (manual pulser) | MDR (drive switch) |

PA, PB: Input signals from a manual pulser.
A motor can be operated in synchronization with a manual pulser.
PA/PB signal input specifications can be selected by the software: 2-pulses or 90-degree phase difference (1x, 2x or 4x) by using RENV2.PIM bit.

PDR, MDR: Input the signal from a drive switch.
A motor can be operated only while the drive switch is ON, or it can be operated only by a certain amount every time the drive switch is ON.
The input logic can be selected using RENV1.DRL bit.

Noise filters can be inserted into PA/PDR and PB/MDR terminals using RENV2.PINF bit.
The states of PA and PB terminals can be monitored by RSTS.SPA bit and RSTS.SPB bit.

## 3.3.8 A0/PS0 [44], A1/PS1 [45], PS2 [46], PS3 [47], PS4 [48]

In stand-alone operation system (MODE = H), the terminals become PS0 to PS4 for selecting an operation pattern. In CPU-connected system (MODE = L), the terminals become A0 and A1 for LSI selection.
In either case, the input logic is positive. (0: L level, 1: H level)

| Setting / Terminal name | MODE = L-level (CPU-connected system ) | MODE = H-level (Stand-alone operation system ) |
|---|---|---|
| A0/PS0 | A0: LSI selection 0 | PS0: Operation pattern setting 0 |
| A1/PS1 | A1: LSI selection 1 | PS1: Operation pattern setting 1 |
| PS2 | (*) | PS2: Operation pattern setting 2 |
| PS3 | (*) | PS3: Operation pattern setting 3 |
| PS4 | (*) | PS4: Operation pattern setting 4 |

Select the LSI whose setting value of LSI selection is the same as bits 5 and 4 of the bus control command to perform serial communication. Therefore, up to four LSIs can be connected to one set of serial buses.

(*) : Be sure to pull down (5 kΩ to 10 kΩ).
When input level changes during operation, an emergency stop occurs and RCUN register (current position counter) is reset.
Even in a stand-alone operation, an emergency stop occurs when the input levels of PS0 to PS4 terminals change during an operation.

## 3.3.9 EA [11], EB [12], EZ [13]

EA and EB terminals are for encoder signal input:
The input specification is specified by RENV2. EIM bit. The input specification can be selected from either 2-pulse input or 90-degree phase differences (1x, 2x or 4x) input.
EZ terminal is an input terminal for encoder Z-phase signal, and it can be used in the operation mode for origin return.
Each terminal can be monitored by RSTS.SEA bit, RSTS.SEB bit or RSTS.SEZ bit.

## 3.3.10 BSY/END [20]

Output a signal indicating that an operation is in progress or is completed. It functions as shown below depending on RENV1.ENDM bits.

| Setting / Terminal name | RENV1.ENDM = 0 | RENV1.ENDM = 1 |
|---|---|---|
| BSYEND | BSY (During operation) | END (Operation completed) |

BSY: Outputs L level during operation and returns to H level upon end of the operation.
END: Outputs L level when an operation is ended with “STA = L level”, and returns to H level by setting STA = H level.
For the difference between BSY and END signals, see “10.2 Operation status check output”

## 3.3.11 SD [15]

Input terminal for deceleration signals:
RMD.MSDE bit allows you to select either this signal is enabled or disabled. Input logic can be selected by RENV1.SDL bit.
RENV1.SDM bit allows you to select either “decelerate” or “decelerate and stop” when this signal is ON.
When “decelerate” is selected, deceleration starts when SD signal is turned ON, and it accelerates again when SD signal turns OFF again.
When deceleration stop is selected, it accelerates again if it returns to OFF during deceleration. If deceleration stop is selected, it remains stopped even if it returns to OFF after stopping.

If the latch function is enabled by “RENV1.SDLT = 1”, deceleration stop can be performed even if spike-shaped signals are input. The input state is latched at start, and thereafter the change from input OFF to ON will be stored.

SD terminal status can be monitored by RSTS.SSD bit.
Latching state of SD signal can be monitored by RSTS.SDIN bit.

## 3.3.12 PELL [22], MELL [21]

Terminals to set the input logic of EL signal through hardware.
Select the logic of PEL signal by PELL terminal, and select the logic of MEL signal by MELL terminal.

| ELL terminal | Operation |
|---|---|
| L | Input of EL signal operates with positive logic. |
| H | Input of EL signal operates with negative logic. |

## 3.3.13 PEL [17], MEL [16]

Input terminals for EL signals. Input logic can be specified by PELL, MELL terminals.
When EL signal in the moving direction turns ON, the operation stops immediately. Even if returning to OFF, the operation remains stopped.
When EL signal in the moving direction is ON at start, the stop state is maintained.
When timer is selected as the operation mode, EL signal is disabled.
EL terminal state can be monitored by RSTS.SPEL bit and RSTS.SMEL bit.

## 3.3.14 ORG [14]

As for input terminal for origin signal, input logic can be specified by RENV1.ORGL bit.

When the operation mode is origin return (RMD.MOD = 1h, 2h), the operation stops immediately when ORG signal changes from OFF to ON. After that, the operation remains stopped even if this signal returns to OFF.
Please note that operation will never stop if you start with ORG signal ON.

When the operation mode is origin escape (RMD.MOD = 3h), the operation stops immediately when ORG signal turns OFF. After that, the operation remains stopped even if the signal returns to ON.
Also, if you start with ORG signal OFF, the stop state is maintained.

ORG terminal state can be monitored by RSTS.SORG bit.

## 3.3.15 STA [42]

I/O terminal for external starts
An external start requires an external pull-up resistor.
When “RMD.MSY = 1” is set, an operation starts at the falling edge of STA signal after a start command is input.
Be sure to drive the external circuit with an open drain.
Signals less than 5 cycles of the reference clock are not accepted.
Writing STAO commands enables to output one-shot pulse.
STA terminal state can be monitored by RSTS.SSTA bit.
See “10.7 External start and simultaneous start” for details.

## 3.3.16 STP [43]

Input terminal for an external stop.
Input logic can be selected with RENV1.STPL bit.
Use RMD.MSPE bit to specify whether STP signal is abled or disabled.
RENV1.STPM bit is used to select either “immediate stop” or “deceleration stop” by STP signal.
Even if this signal returns to OFF after stopping, it remains stopped.
If STP signal is ON at start, the operation does not start.
STP terminal state can be monitored by RSTS.SSTP bit.
See “10.8 External stop” for details.

## 3.3.17 OUT/PH1 [26], DIR/PH2 [27]

With MTYP terminal, they function as follows:

| Setting / Terminal name | MTYP = L (Pulse train output mode) | MTYP = H (Excitation sequence output mode) |
|---|---|---|
| OUT/PH1 | OUT output | PH1 output |
| DIR/PH2 | DIR output | PH2 output |

OUT, DIR: Pulse output terminal for driving a motor.
RENV1.PMD bit allows you to specify from eight types of output specification.
Mask the pulse output when the operation mode is “positioning control - timer”. Direction signal is output.

PH1, PH2: Phase signal for stepping motors is output.
Phase distribution signal for stepping motors is output together from P2/PH3 and P3/PH4 terminals.
Output mode changes depending on UB and FH terminals.
PH1 to PH4 terminal status can be monitored by RSTS.SPH bit.
Excitation sequence is not switched when Operation mode is “positioning control - timer”.

## 3.3.18 ERC/CDW [19]

The following signals can be specified by RENV1.CDWS bit.

| Setting / Terminal name | CDWS = 0 | CDWS = 1 |
|---|---|---|
| ERC/CDW | ERC output | CDW output |

ERC: Deviation counter clear signal is output for servo motor system.
CDW: Current down signal is output for stepping motors.

ERC/CDW signal logic can be changed by RENV1.ERCL bit.
ERC/CDW terminal state can be monitored by RSTS.SERC bit.

## 3.3.19 UB [24]

Input terminal to set the drive mode.
UB terminal state can be monitored by RSTS.SPUB bit.

| UB terminal | Operation |
|---|---|
| L | Outputs excitation sequence of unipolar drive from PH1 to PH4 terminals. |
| H | Outputs excitation sequence of bipolar drive from PH1 to PH4 terminals. |

When pulse train output mode (MTYP = L) is selected, connect with pull-down (5 kΩ to 10 kΩ), unconnected or connect directly to GND.

## 3.3.20 INP/FH [23]

Depending on MTYP input terminal state, the terminal function is as follows:

| Setting / Terminal name | MTYP = L (Pulse train output mode) | MTYP = H (Excitation sequence output mode) |
|---|---|---|
| FH/INP | INP input | FH input |

INP: Input terminal for in-position signal (=positioning complete signal).
Input signal from a servo motor driver.
You can set operation complete when the motor stops after pulse output is completed.
Signal logic can be changed by RENV1.INPL bit. Terminal state can be monitored by RSTS.SINP bit.

FH: Terminal to set the excitation method.
Select the excitation method for 2-phase stepping motor; full step or half step.
Full step at L level; half step at H level.

## 3.3.21 P0 [1], P1 [2]

General-purpose I/O terminals used in CPU-connected system.
RIOP.PMD bit allows I/O selection on bit-by-bit basis.

Be sure to pull down (5 kΩ to 10 kΩ) in stand-alone operation system (MODE = H level),

## 3.3.22 P2/PH3 [28], P3/PH4 [29]

Depending on MTYP terminal, terminal functions are as follows:

| Setting / Terminal name | MTYP = L (Pulse train output mode) | MTYP = H (Excitation sequence output mode) |
|---|---|---|
| P2/PH3 | General-purpose output terminal P2 | Phase signal output PH3 |
| P3/PH4 | General-purpose output terminal P3 | Phase signal output PH4 |

General-purpose output terminals (P2, P3): General-purpose output terminals.

Phase signal output PHn: Output terminal of stepping motor excitation signal.
Excitation sequence signal switches in synchronization with output pulse.
Full step or half step of excitation sequence can be selected by F/H terminal.
Unipolar drive or bipolar drive of excitation sequence can be selected by U/B terminal.
When the operation mode is set as “positioning control - timer”, the excitation sequence does not change.

Be sure to pull down (5 kΩ to 10 kΩ) when pulse train mode (MTYP = L level) is used in stand-alone operation system (MODE = H level).

## 3.3.23 VDD [8, 30, 41], GND [6, 18, 25, 31, 32, 37, 39]

Input terminal of power supply.
Input +3.3 V ± 0.3 V to VDD.
Be sure to connect all terminals.

# 4. Memory map

The control registers are deployed over the memory map and can be accessed from CPU in the same way as memory access.
The most frequently used registers are located near the command register (RCOM).
Therefore, the writing time can be shortened by a block writing process. (One block can process all registers.)

| Address | Register name | Attribute | Bit-length | Description |
|---|---|---|---|---|
| 04h to 07h | RENV2 | R/W | 32 | Environment setting 2 |
| 08h to 0Bh | RENV1 | R/W | 30 | Environment setting 1 |
| 0Ch, 0Dh | RDS | R/W | 12 | Deceleration S-curve section |
| 0Eh, 0Fh | RUS | R/W | 12 | Acceleration S-curve section |
| 10h, 11h | RDR | R/W | 16 | Deceleration rate |
| 12h, 13h | RUR | R/W | 16 | Acceleration rate |
| 14h, 15h | RMG | R/W | 12 | Speed magnification |
| 16h to 18h | RDP | R/W | 24 | Slow-down point |
| 19h, 1Ah | RFL | R/W | 13 | FL speed (initial speed) step value |
| 1Bh, 1Ch | RFH1 | R/W | 13 | FH1 speed (operation speed) step value |
| 1Dh, 1Eh | RFH2 | R/W | 13 | FH2 speed (operation speed) step value |
| 1Fh to 22h | RMV | R/W | 28 | Number of output pulses |
| 23h, 24h | RMD | R/W | 15 | Operation mode |
| 25h | RCOM | R/W | 8 | Command |
| 26h to 29h | RSTS | R | 32 | Status |
| 2Ah, 2Bh | RIST | R/W | 16 | Interrupt factor register |
| 2Ch, 2Dh | RIOP | R/W | 16 | General-purpose I/O terminal control |
| 2Eh to 31h | RCUN | R/W | 32 | Current position counter |
| 32h to 35h | RDWC | R | 28 | Number of remaining pulses |
| 36h, 37h | RSPD | R | 13 | Current speed monitor |

When multiple bytes are written in serial communication, they are written into the register one byte at a time. The all bytes in a register cannot be changed at a time.

RFH1 and RFH2 registers of FH speed setting are intended for the target speed override during operation.
To perform the target speed override while operating at FH1 speed, set a new speed in FH2 register, first.
Then, the target speed is overridden to FH2 speed by speed change command.

# 4.1 Detailed memory map

| Address | Description (8 bit) | |
|---|---|---|
| 00 | Reserved * | Reserved (access prohibited) |
| 01 | Reserved * | |
| 02 | Reserved | |
| 03 | Reserved | |
| 04 | RENV2 (31~24) | Environment setting 2 |
| 05 | RENV2 (23~16) | |
| 06 | RENV2 (15~08) | |
| 07 | RENV2 (07~00) | |
| 08 | RENV1 (31~24) | Environment setting 1 |
| 09 | RENV1 (23~16) | |
| 0A | RENV1 (15~08) | |
| 0B | RENV1 (07~00) | |
| 0C | RDS (15~08) | S-curve section for deceleration specification |
| 0D | RDS (07~00) | |
| 0E | RUS (15~08) | S-curve section for acceleration specification |
| 0F | RUS (07~00) | |
| 10 | RDR (15~08) | Deceleration rate |
| 11 | RDR (07~00) | |
| 12 | RUR (15~08) | Acceleration rate |
| 13 | RUR (07~00) | |
| 14 | RMG (15~08) | Speed magnification |
| 15 | RMG (07~00) | |
| 16 | RDP (23~16) | Slow-down point |
| 17 | RDP (15~08) | |
| 18 | RDP (07~00) | |
| 19 | RFL (15~08) | Initial speed (FL) |
| 1A | RFL (07~00) | |
| 1B | RFH1 (15~08) | Operating speed 1 (FH1) |
| 1C | RFH1 (07~00) | |
| 1D | RFH2 (15~08) | Operating speed 2 (FH2) |
| 1E | RFH2 (07~00) | |
| 1F | RMV (31~24) | Number of output pulses (=feeding amount) |
| 20 | RMV (23~16) | |
| 21 | RMV (15~08) | |
| 22 | RMV (07~00) | |
| 23 | RMD (15~08) | Operation mode |
| 24 | RMD (07~00) | |
| 25 | RCOM (07~00) | Command |
| 26 | RSTS (31~24) | Status |
| 27 | RSTS (23~16) | |
| 28 | RSTS (15~08) | |
| 29 | RSTS (07~00) | |
| 2A | RIST (15~08) | Interrupt factor |
| 2B | RIST (07~00) | |
| 2C | RIOP (15~08) | General-purpose I/O terminal control |
| 2D | RIOP (07~00) | |
| 2E | RCUN (31~24) | Current position counter |
| 2F | RCUN (23~16) | |
| 30 | RCUN (15~08) | |
| 31 | RCUN (07~00) | |
| 32 | RDWC (31~24) | Number of remaining pulses |
| 33 | RDWC (23~16) | |
| 34 | RDWC (15~08) | |
| 35 | RDWC (07~00) | |
| 36 | RSDP (15~08) | Current speed |
| 37 | RSDP (07~00) | |
| 38 | - | Unused |
| 39 | - | |
| 3A | - | |
| 3B | - | |
| 3C | - | |
| 3D | - | |
| 3E | - | |
| 3F | - | |

*: Addresses “00” and “01” are used in ID monitor. See “10.10 ID monitor” for details.

# 5. Serial communication format

PCD2112A is a slave dedicated LSI for 4-wire serial communication.
Set CPU as a master.
One communication starts when CPU changes CS terminal from H to L level.
When CS terminal becomes H level, the communication is terminated.
There are seven types of communication formats for one communication as follows:

1) Read register values from PCD2112A
   (bus control command: 1 byte) + (start address: 1 byte) + (read data: several bytes)

2) Write register values to PCD2112A
   (bus control command: 1 byte) + (start address: 1 byte) + (write data: several bytes)

3) Read bus status
   (bus control command: 1 byte) + (status read value: 1 byte)

4) Write access control to EEPROM for stand-alone operation
   (bus control command: 1 byte)

5) Read data from EEPROM for stand-alone operation.
   (EEPROM command: 1 byte) + (start address: 2 bytes) + (read data: several bytes)

6) Write data to EEPROM for stand-alone operation.
   (EEPROM command: 1 byte) + (start address: 2 bytes) + (write data: several bytes)

7) Read status from EEPROM for stand-alone operation.
   (EEPROM command: 1 byte) + (status read value: 1 byte)

## 5.1 Bus control command

PCD2112A is controlled by 4-wire serial bus, but the access to PCD2112A is half-duplex communication.
The bus-control command distinguishes whether this serial communication is “Read”, “Write” or “Other”.

**Table 5.1-1 Bus control command list**

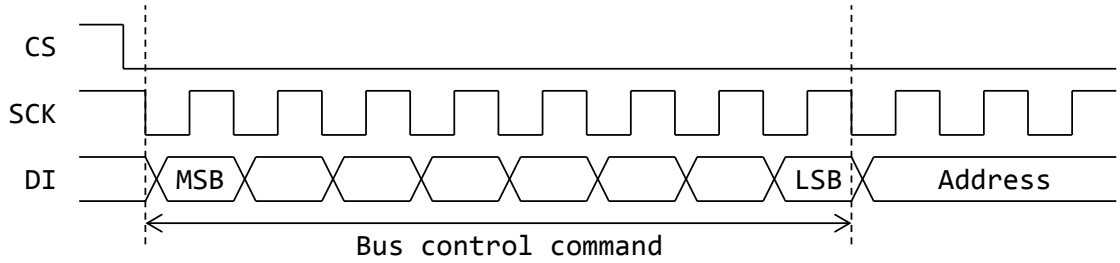
| Command | Code | Description |
|---|---|---|
| READ | 00nn 0011b | Read from PCD2112A |
| WRITE | 00nn 0010b | Write to PCD2112A |
| RDSR | 00nn 0101b | Read bus status |
| WREN | 00xx 0110b | Shift to EEPROM access mode |
| WRDI | 00xx 0100b | Exit EEPROM access mode |

PCD2112A has A1 and A0 terminals for LSI number selection and up to four pcs of “PCD2112A” can be connected with one CS signal.
“nn” in the code field of “Table 5.1-1 Bus control command list” sets the LSI number to be accessed.
“Bit 5 = 0” if “A1 = L level” and “Bit 4 = 1” if “A0 = H level”.
When controlling multiple LSIs with one CS signal, see “5.9 Multiple LSI connections”.

“xx” in the code field in “Table 5.1-1 Bus control command list” shows “Don't care”.

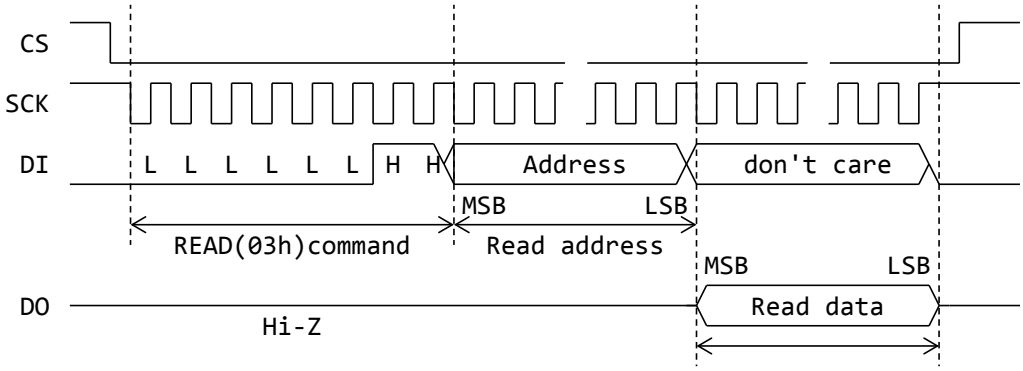
## 5.2 Basic operations

Serial bus basic operation starts at the falling edge of CS signal as follows.
After CS signal falls, DI signal is fetched in synchronization with the rising edge of SCK signal.
Specify “Bus control command” in the first 8 bits.



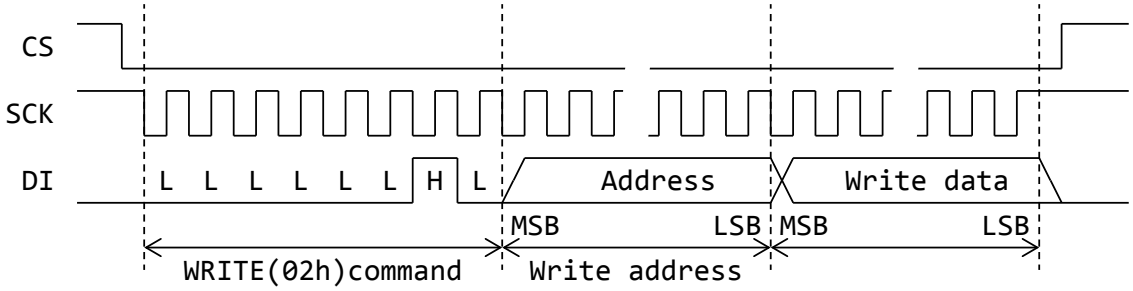

## 5.3 Read operation from PCD2112A

When CPU sends READ (03h) command and read address (8 bit), PCD2112A outputs read data from the specified starting address in synchronization with the falling edge of SCK signal.
The read data is output in 8 bit units.
If SCK signal is continuously input while “CS = L level” is maintained, the data can be read continuously while adding addresses one by one.
The read data is latched after writing READ (03h) command.
Even if the current speed, current position, etc. are changed during reading, output read data will be the data at the time of latching.
Read data becomes 00h when read from undefined addresses (00h to 03h, 38h to 3Fh).




## 5.4 Write operation to “PCD2112A”

When WRITE (02h) command, write addresses (8 bit), and the data to write are sent from CPU in this order, PCD2112A fetches them at the rising edge of SCK signal. PCD2112A fetches write data in 8 bit units.
If SCK signal is continuously input while “CS = L level” is maintained, the data can be written continuously while adding addresses one by one.
PCD2112A writes 8 bit data to the specified address in synchronization with CLK signal every sampling.
Since PCD2112A manages the write address with an 8-bit write address counter, PCD2112A has the same address in 256 byte cycles.
Writing to undefined addresses (00h to 03h, 38h to 3Fh) is ignored.



# 5.5 Reading bus status operation

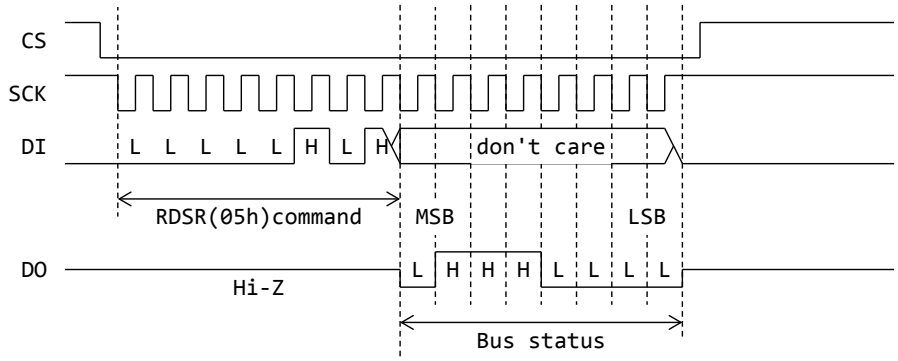
This operation is used to check when accessing EEPROM for Stand-alone operation system.
After WREN (06h) command is written, the communication target of CPU is EEPROM.
After WRD (04h)I command is written, the command returns to PCD2112A.
Read the bus status to determine which the current target of communication is.
If RDSR (05h) command is sent when the communication target is PCD2112A, the bus status can be read out in synchronization with SCK signal.
When PCD2112A is the target, bits 6 to 4 of bus status become “111”. When EEPROM is the target, check the EEPROM specifications. See “11.2 Data-setting to EEPROM” for details.

Note: In the EEPROM where bits 6 to 4 of bus status are “XXX”, reading of the bus status cannot be checked.

Bus status when PCD2112A is the target:

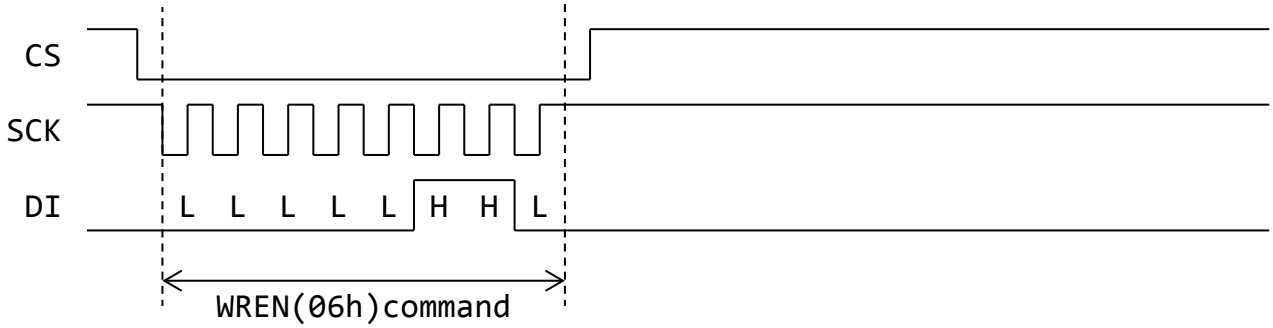
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Timing:



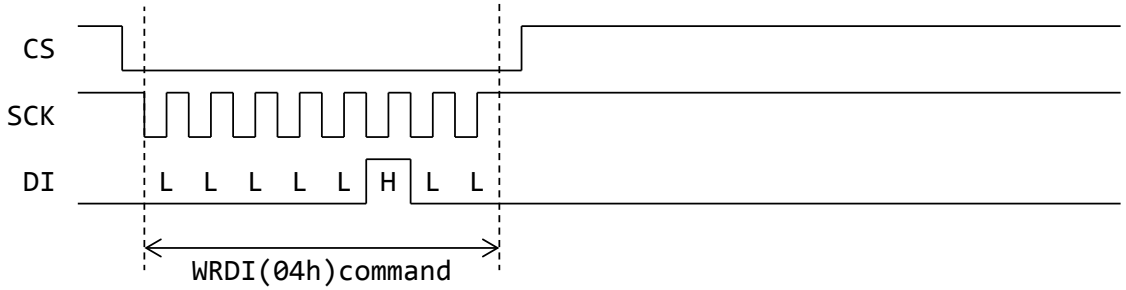

# 5.6 Transition to EEPROM access mode

In stand-alone operation, CSO terminal output of PCD2112A is connected to CS terminal of EEPROM.
Immediately after the power is turned ON, CSO terminal output of PCD2112A becomes “H level”.
“CSO = H level” means that CPU cannot access EEPROM.
When WREN (06h) command is transmitted from CPU, CS signal input to “PCD2112A” is output from CSO terminal.
The serial communication target from CPU is EEPROM during EEPROM access mode, so PCD2112A does not accept commands other than WRDI command.



# 5.7 Terminating EEPROM access mode

This operation is used to check when accessing EEPROM in Stand-alone operation system.
Only WRDI (04h) command is accepted even when PCD2112A is in EEPROM access mode.
EEPROM access mode ends immediately after receiving this command, and PCD2112A is fixed to “CSO = H level”.
Thereafter, the communication target returns to PCD2112A.




WRDI command 04h is defined as a “write disable” command in EEPROM specification.
Therefore, when this WRDI command is written, PCD2112A exits EEPROM access mode, so that EEPROM is disabled to be written.

# 5.8 EEPROM control

To access EEPROM from CPU, temporarily switch to CPU connection system and change EEPROM contents.
See “2.5.2 Stand-alone operation system (MODE = H)” for details.
For EEPROM that can be used in Stand-alone operation system, please meet “11.1 EEPROM selection criteria”.

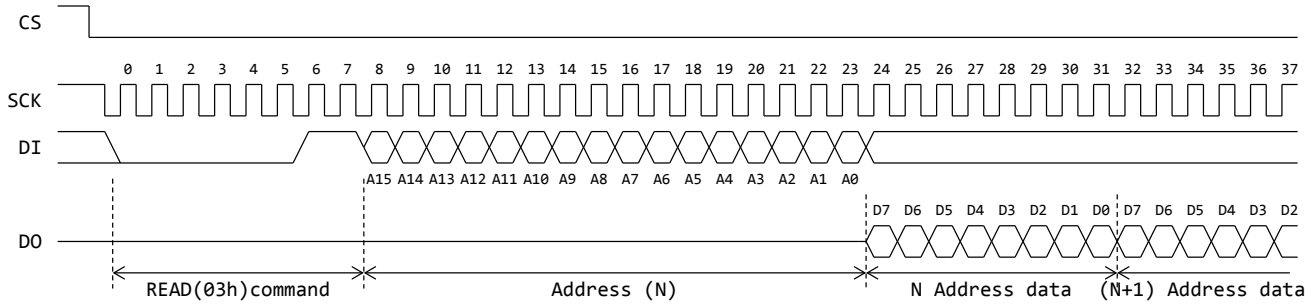



**Fig. 5.8-1 EEPROM reading timing in Stand-alone operation system**

Note: In Stand-alone operation system, DI terminal becomes an output terminal and DO terminal becomes an input terminal.

After PCD2112A enters EEPROM access mode, refer to the EEPROM manual to be used for writing.

Note: To enable EEPROM, PCD2112A should be set to EEPROM access mode.
Then “Enable writing” commands need to be written; (i.e., “00000110” is written twice).

Procedures to write from CPU to EEPROM:

1) Send bus control command WREN (06h) to set EEPROM access mode.
2) Send EEPROM control command, WREN (06h) to put EEPROM in the writable state.
3) EEPROM control commands WRITE (02h), 16 bit writing addresses, and the data to write are sent in this order and written to EEPROM.
   Note that the number of bytes that can be written at one time varies depending on the EEPROM to use, so they need to written separately in several times.
   For address maps in EEPROM, see “11 Supplementary description of Stand-alone operation system“.
4) Send bus control command, WRDI (04h).
   This command communication is received by EEPROM and “PCD2112A”, and EEPROM access mode completed at the same time that EEPROM is in the write protected state.

# 5.9 Multiple LSI connections

PCD2112A has 2 bit of LSI number setting terminals; (A0, A1).
They are enabled only in CPU-connected system.
Four “PCD2112A” can be multi-drop connected to one CS signal.
The LSI number (A0, A1) is specified by bit 4 and 5 of bus control command.

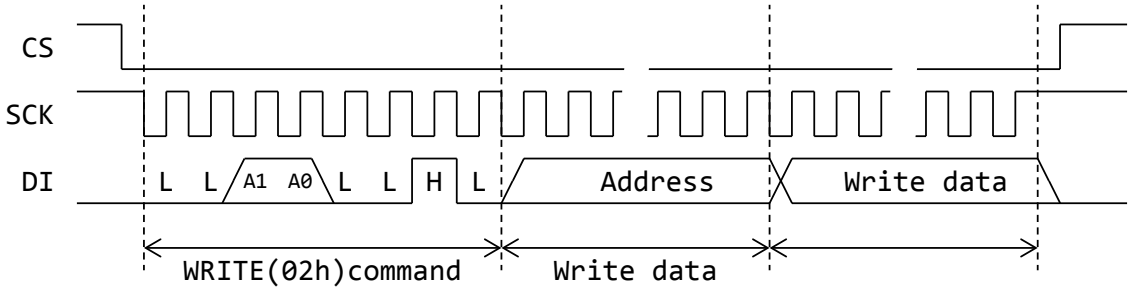



**Fig. 5.9-1 Example of bus control command when LSI number (A0, A1) is used.**

# 6. Commands

The values written to RCOM register becomes “Commands”.
Do not write any codes other than the following to RCOM register:

**Table 6-1 Command list**

| Code | Name | Content |
|---|---|---|
| 00h | NOP | Invalid |
| 01h | SRST | Software reset (*) |
| 03h | IDMON | ID code confirmation command |
| 05h | SRDS | Disable SRST command (default ) |
| 0Ah | SREN | Enable SRST command |
| 10h | ERCO | ERC signal output |
| 11h | ERCR | ERC signal output stop |
| 12h | STAO | STA output |
| 13h | CUNR | Current position counter clear to zero (=zero-clear command) |
| 14h | TRST | Direction change timer reset |
| 30h | EMGSP | Emergency stop |
| 31h | STOP | Immediate stop |
| 32h | SDSTP | Deceleration stop |
| 40h | STAFL | FL constant speed start |
| 41h | STAFH1 | FH1 constant speed start |
| 42h | STAFH2 | FH2 constant speed start |
| 43h | STAUD1 | Start with acceleration/deceleration (FL→FH1) |
| 44h | STAUD2 | Start with acceleration/deceleration (FL→FH2) |
| 50h | CNTFL | FL constant speed remaining pulse start |
| 51h | CNTFH1 | FH1 constant speed remaining pulse start |
| 52h | CNTFH2 | FH2 constant speed remaining pulse start |
| 53h | CNTUD1 | Accel/decel remaining pulse start (FL→FH1) |
| 54h | CNTUD2 | Accel/decel remaining pulse start (FL→FH2) |
| 60h | FCHGL | Immediate speed change to FL speed |
| 61h | FCHGH1 | Immediate speed change to FH1 speed |
| 62h | FCHGH2 | Immediate speed change to FH2 speed |
| 63h | FSCHL | Decelerate to FL speed |
| 64h | FSCHH1 | Accelerate/decelerate to FH1 speed |
| 65h | FSCHH2 | Accelerate/decelerate to FH2 speed |

Note: Write “Start command” while “RSTS.SCM=0000b” (operation is being stopped).
Operations cannot be guaranteed if the data is written while not being stopped.

* : Write SREN (0Ah) command before writing SRST (01h) command.
Write SRDS (05h) command after writing SRST (01h) command.
Be sure to reset by RST signal after turning ON the power.
All commands including SRST (01h) command may not be accepted.

# 6.1 Operation command

## 6.1.1 Start command

| RCOM | Name | Description |
|---|---|---|
| 40h | STAFL | Constant-speed start at FL speed.<br>Speed pattern is in FL constant-speed pattern. |
| 41h | STAFH1 | Constant-speed start at FH1 speed.<br>Speed pattern is in FH1 constant-speed pattern. |
| 42h | STAFH2 | Constant-speed start at FH2 speed.<br>Speed pattern is in FH2 constant-speed pattern. |
| 43h | STAUD1 | High-speed start from FL speed.<br>Speed pattern is in FH1 high-speed pattern. |
| 44h | STAUD2 | High-speed start from FL speed.<br>Speed pattern is in FH2 high-speed pattern. |

## 6.1.2 Remaining-pulse start command

| RCOM | Name | Description |
|---|---|---|
| 50h | CNTFL | RDWC register value is not reset, and it operates similar to STAFL (40h) command. |
| 51h | CNTFH1 | RDWC register value is not reset, and it operates similar to STAFH1 (41h) command. |
| 52h | CNTFH2 | RDWC register value is not reset, and it operates similar to STAFH2 (42h) command. |
| 53h | CNTUD1 | RDWC register value is not reset, and it operates similar to STAUD1 (43h) command. |
| 54h | CNTUD2 | RDWC register value is not reset, and it operates similar to STAUD2 (44h) command. |

The remaining-pulse start command is a command to continue operation for remaining pulses when positioning control is interrupted.

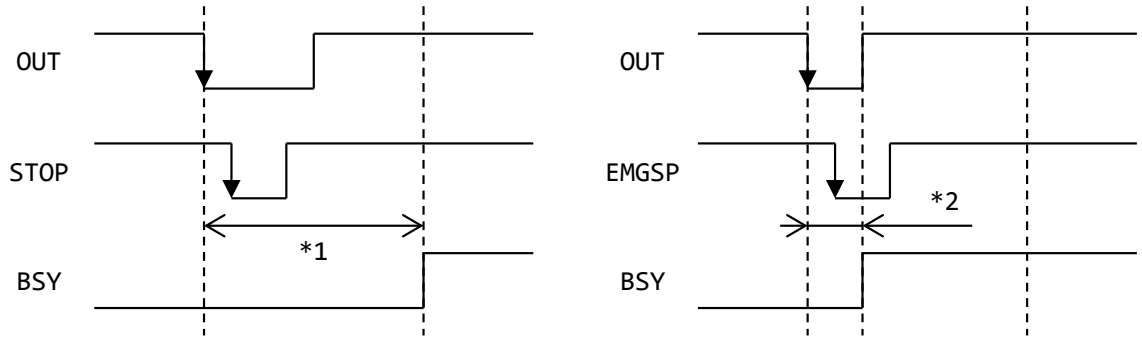
## 6.1.3 Speed-change command

| RCOM | Name | Description |
|---|---|---|
| 60h | FCHGL | Change to FL speed instantaneously. |
| 61h | FCHGH1 | Change to FH1 speed instantaneously. |
| 62h | FCHGH2 | Change to FH2 speed instantaneously. |
| 63h | FSCHL | Decelerate and change to FL speed. |
| 64h | FSCHH1 | Change to FH1 speed by accelerating or decelerating. |
| 65h | FSCHH2 | Change to FH2 speed by accelerating or decelerating. |

Speed-change command cannot be used in switch control mode and manual pulser-control operation mode.

## 6.1.4 Stop command

| RCOM | Name | Description |
|---|---|---|
| 30h | EMGSP | Emergency stop. It stops even in the middle of the last pulse. |
| 31h | STOP | Immediate stop. It stops after the last pulse output is completed. |
| 32h | SDSTP | Decelerate and stop. |




*1: STOP (31h) command can secure the final pulse cycle.
*2: EMGSP (30h) command cannot secure even the final pulse width.
If the last pulse is spiked-shape, the motor driver may not accept it; in this case, RCUN register value may not match with a mechanical position.

# 6.2 Control command

## 6.2.1 Software reset command

| RCOM | Name | Description |
|---|---|---|
| 01h | SRST | Software reset. |
| 05h | SRDS | Disable SRST command. |
| 0Ah | SREN | Enable SRST command. |

## 6.2.2 Counter zero-clear command

| RCOM | Name | Description |
|---|---|---|
| 13h | CUNR | Clear the current position counter to zero. |

## 6.2.3 ERC signal output control command

| RCOM | Name | Description |
|---|---|---|
| 10h | ERCO | Outputs ERC signal. |
| 11h | ERCR | Resets output when ERC signal output is set to level output. |

Note : This command is ignored when MTYP terminal is at “H level” (excitation sequence output).

## 6.2.4 STA signal output control command

| RCOM | Name | Description |
|---|---|---|
| 12h | STAO | Outputs a one-shot signal of 0.8 μs width from STA terminal. |

## 6.2.5 Other commands

| RCOM | Name | Description |
|---|---|---|
| 00h | NOP | No effect to operations. |
| 03h | IDMON | Sets ID code to addresses “00” and “01”. |
| 14h | TRST | Resets a direction change timer. |

# 7. Registers

## 7.1 RMD: Operation mode setting register

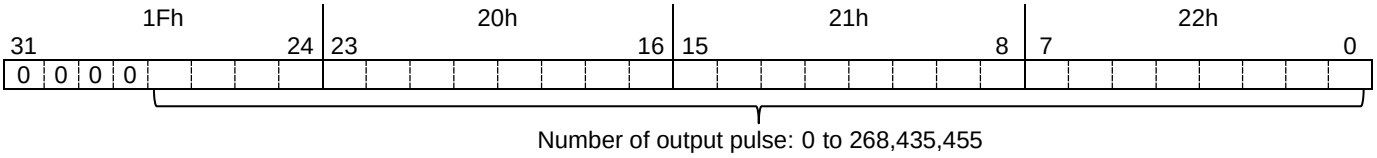
The following is the table of registers to set operation modes: [Address: 23h to 24h]

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | MSY | MSPE | MADJ | MINP | MCCE | MSDP | MSDE | MSMD | MDIR | MOD | | | |

| Address | Bit | Name | Description |
|---|---|---|---|
| 24h | 3~0 | MOD | Operation mode<br>0000: Command control – Continuous movement<br>0001: Origin signal control – Origin return movement<br>0010: Origin return movement with feeding amount limit<br>0011: Origin signal control – Origin scape<br>0100: EL signal control – EL escape<br>0101: Positioning control – incremental movement<br>0110: Positioning control – timer<br>0111: Switch control – continuous movement<br>1000: Switch control incremental movement<br>1001: Pulser-control continuous movement<br>1010: Pulser-control incremental movement<br>1011: Setting prohibited<br>1100: Setting prohibited<br>1101: Setting prohibited<br>1110: Setting prohibited<br>1111: Setting prohibited |
| | 4 | MDIR | Moving direction<br>0: Positive (= +) direction.<br>1: Negative (= −) direction.<br>This function is not used in switch control operation mode.<br>Also not used in operations of incremental movement with manual pulser. |
| | 5 | MSMD | Acceleration/deceleration characteristics<br>0: Linear acceleration/deceleration.<br>1: S-curve acceleration/deceleration. |
| | 6 | MSDE | SD (=Slow-down) signal input<br>0: Disable.<br>1: Enable (Decelerate / decelerate and stop). |
| | 7 | MSDP | Slow-down point setting<br>0: Automatic setting.<br>1: Manual setting. |
| 23h | 8 | MCCE | Remaining-pulse number counter (RDWC register)<br>0: Run.<br>1: Stop.<br>When “RENV2.CUNI = 0”, current position counter (RCUN register) also stops.<br>When “RENV2.CUNI = 1”, only current position counter (RCUN register) runs.<br>When “RMD.MCCE = 1”, the machine position can be corrected without changing the number of remaining pulses. |
| | 9 | MINP | INP signal input<br>0: Disabled.<br>1: Enabled (Wait for positioning completion signal). |
| | 10 | MADJ | Triangle drive avoidance<br>0: Enabled.<br>1: Disabled.<br>When “RMD. MSDP = 1”, triangle driving avoidance is disabled even with “RMD.MADJ = 0”. |
| | 11 | MSPE | STP signal input<br>0: Disabled.<br>1: Enabled (deceleration stop or immediate stop). |
| | 12 | MSY | Start timing by writing a start command<br>0: Start immediately.<br>1: Wait for STA signal input. |
| | 13 | - | Must always set to “0”. |
| | 14 | - | Must always set to “0”. |
| | 15 | - | Must always set to “0”. |

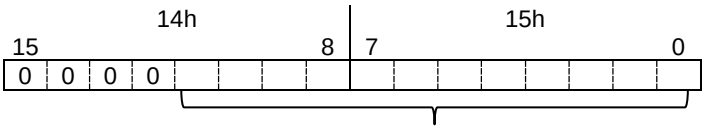
# 7.2 RMV: Number of output pulse setting register

Register to set the number of pulse to output in operation mode of feeding amount limit or incremental movement. [Address: 1Fh to 22h]
The moving direction is set by RMD.MDIR bit.




# 7.3 RMG: Speed magnification setting register

Register to set the speed magnification rate. [Address: 14h to 15h]




$$MG = \frac{CLK[Hz]}{(RMG + 1) \times 8{,}192} \qquad RMG = \frac{CLK[Hz]}{MG \times 8{,}192} - 1$$

MG: Speed magnification

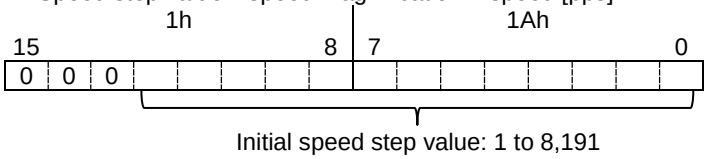
When the reference clock frequency is 9.8304 MHz, the relationship will be shown below:

| Setting value | Speed magnification (MG) | Output speed range (pps) |
|---|---|---|
| 2399 (95Fh) | 0.5 | 0.5 to 4,095.5 |
| 1199 (4AFh) | 1 | 1 to 8,191 |
| 599 (257h) | 2 | 2 to 16,382 |
| 239 (0EFh) | 5 | 5 to 40,955 |
| 119 (077h) | 10 | 10 to 81,910 |

| Setting value | Speed magnification (MG) | Output speed range (pps) |
|---|---|---|
| 59 (03Bh) | 20 | 20 to 163,820 |
| 23 (017h) | 50 | 50 to 409,550 |
| 11 (00Bh) | 100 | 100 to 819,100 |
| 5 (005h) | 200 | 200 to 1,638,200 |
| 3 (003h) | 300 | 300 to 2,457,300 |

# 7.4 RFL: FL speed setting register

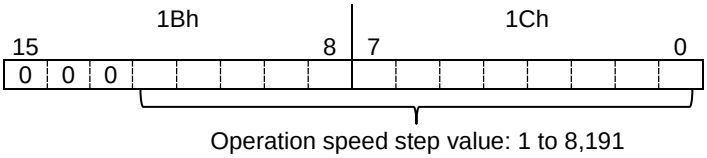
Register to set FL speed (= starting speed, stopping speed) by speed step value. [Address: 19h to 1Ah]
Speed step value x speed magnification = speed [pps].




# 7.5 RFH: FH speed setting register

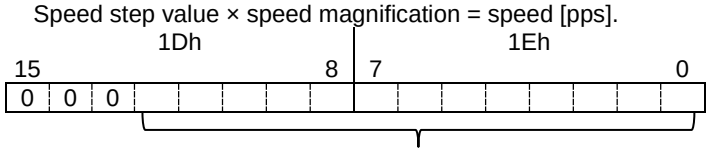
## 7.5.1 RFH1: FH1 speed setting register

Register to set FH1 speed (=operation speed) by speed step value. [Address: 1Bh to 1Ch]
Speed step value x speed magnification = speed [pps].



## 7.5.2 RFH2: FH2 speed setting register

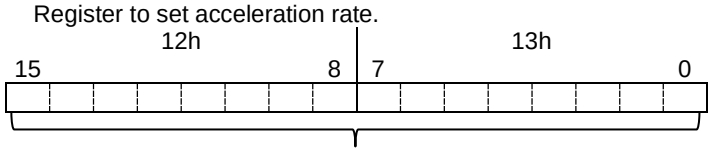
Register to set FH2 speed (=operation speed) by speed step value. [Address: 1Dh to Eh]
Speed step value × speed magnification = speed [pps].




Operation speed step value: 1 to 8,191

## 7.6 RUR: Acceleration rate setting register

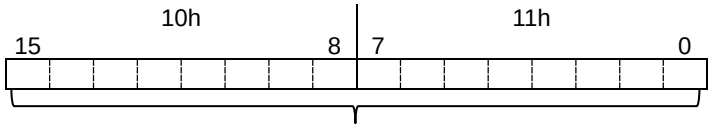
Register to set acceleration rate. [Address: 12h to 13h]




Acceleration rate values: 1 to 65,535

## 7.7 RDR: Deceleration rate setting register

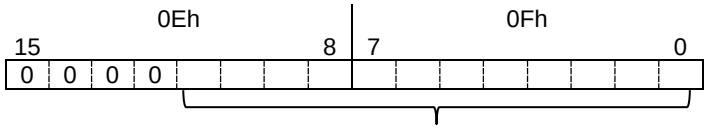
Register to set deceleration rate. [Address: 10h to 11h]
Setting “0” substitutes RUR (=Acceleration rate setting) register value.




Deceleration rate values: 0 to 65,535

## 7.8 RUS: Acceleration S-curve section setting register

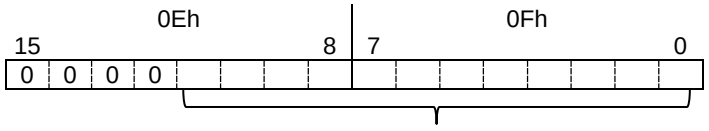
S-curve section of S-curve acceleration is set by speed step value. [Address: 0Eh to 0Fh]
Setting “0” substitutes the value of.$\frac{RFH-RFL}{2}$




Acceleration S-curve section: 0 to 4,095

## 7.9 RDS: Deceleration S-curve section setting register

S-curve section of S-curve deceleration is set by speed step value. [Address: 0Ch to 0Dh]
Setting “0” substitutes the value of $\frac{RFH-RFL}{2}$



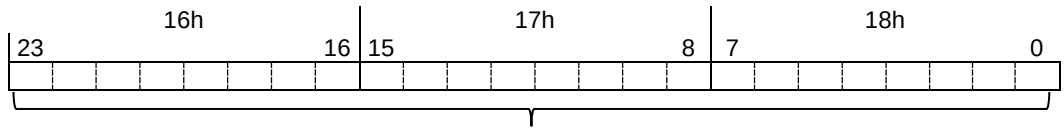

Deceleration S-curve section: 0 to 4,095

# 7.10 RDP: Slow-down point setting register

Register to set slow-down point that can be used in operation mode of incremental movement. [Address: 16h to 18h]
Slow-down point setting method includes automatic setting or manual setting, selectable by RMD.MSDP bit.

When “RMD.MSDP = 0” (automatic setting), slow-down point is automatically calculated during acceleration. Offset for the automatic calculation result is set in RDP register.
Decelerates when “$RDWC\ register\ value \leqq automatic\ calculation\ result + RDP\ register\ value$”
This function can be used when acceleration/deceleration characteristics are symmetrical.

When “RMD.MSDP = 1” (manual setting), RDP register is used to set slow-down point.
Decelerates when “$RDWC\ register\ value \leq RDP\ register\ value$”
Asymmetric acceleration/deceleration characteristics can also be used.
When “RDP = 0” (slow-down point “0”) is set in “RMD.MSDP = 1” (Manual setting), operation stops immediately without decelerating.




Offset: −8,388,608 to + 8,388,607
Slow-down point :0 to 16,777,215

# 7.11 RENV1: Environment setting 1 register

Register to set the environment 1. [Address: 08h to 0Bh]
Sets mainly the specifications of I/O terminals.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSKP | IDL | | | PHMA | PHMK | EROR | EROE | CDWS | ETW | | | ERCL | EPW | | |

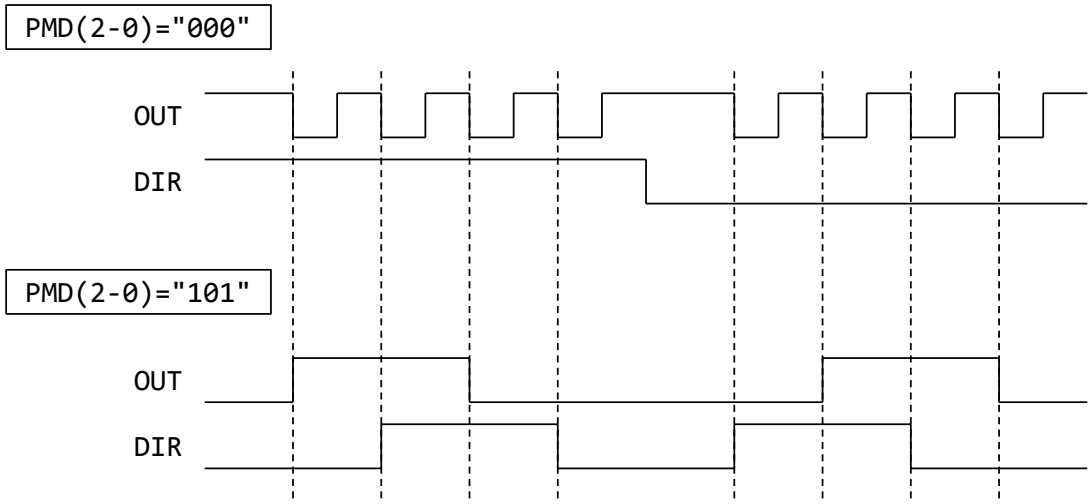
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTMF | ENDM | STAM | FLTR | INPL | DRL | STPL | STPM | ORGL | SDL | SDLT | SDM | ELM | PMD | | |

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0Bh</td><td>2 to 0</td><td>PMD</td><td>
Output pulse mode
<table>
<tr><th rowspan="2">PMD</th><th colspan="2">Positive(=Plus) direction operation</th><th colspan="2">Negative(=Minus) direction operation</th></tr>
<tr><th>OUT output</th><th>DIR output</th><th>OUT output</th><th>DIR output</th></tr>
<tr><td>000</td><td></td><td>High</td><td></td><td>Low</td></tr>
<tr><td>001</td><td></td><td>High</td><td></td><td>Low</td></tr>
<tr><td>010</td><td></td><td>Low</td><td></td><td>High</td></tr>
<tr><td>011</td><td></td><td>Low</td><td></td><td>High</td></tr>
<tr><td>100</td><td></td><td>High</td><td>High</td><td></td></tr>
<tr><td>101</td><td colspan="2">OUT<br>DIR</td><td colspan="2">OUT<br>DIR</td></tr>
<tr><td>110</td><td colspan="2">OUT<br>DIR</td><td colspan="2">OUT<br>DIR</td></tr>
<tr><td>111</td><td></td><td>Low</td><td>Low</td><td></td></tr>
</table>
When it is 101 or 110, it corresponds to 4x only. *
</td></tr>
</table>

| Address | Bit | Name | Description |
|---|---|---|---|
| | 3 | ELM | When EL signal is ON<br>0: Stop immediately.<br>1: Decelerate and stop.<br>Immediately stop when performing constant-speed pattern.<br>When “RENV1.ELM = 1”, EL signal input ON starts deceleration. When the operation stops, EL signal input position has already passed. Be careful not to hit mechanical system, etc. |
| | 4 | SDM | When SD signal is ON<br>0: Decelerate.<br>1: Decelerate and stop. Immediate stop when the speed pattern is a constant speed pattern. |
| | 5 | SDLT | Latch function of SD signal<br>0: Disabled.<br>1: Enabled.<br>Used when SD signal width is short.<br>When SD signal is OFF, latch state will be OFF when an operation starts.<br>Also, even when writing “RENV1.SDLT = 0”, the latching state is turned OFF. |
| | 6 | SDL | Select SD signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| | 7 | ORGL | Select ORG signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| 0Ah | 8 | STPM | When STP signal is ON.<br>0: Decelerate.<br>1: Decelerate and stop. Immediate stop when the speed pattern is a constant speed pattern. |
| | 9 | STPL | Select STP signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| | 10 | DRL | Select PDR signal and MDR signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| | 11 | INPL | Select INP signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| | 12 | FLTR | Input noise filter for PEL, MEL, SD, ORG, and INP terminal.<br>0: Recognize signal width of 0.1 µs or wider.<br>1: Recognize signal width of 4 µs or wider. |
| | 13 | STAM | Select STA signal specification.<br>0: Level trigger.<br>1: Edge trigger. |
| | 14 | ENDM | Select the output signals from BSY/END terminals.<br>0: Outputs BSY signal.<br>1: Outputs END signal. |
| | 15 | DTMF | Direction change timer<br>0: Enabled.<br>1: Disabled.<br>When RENV1.PMD is set to 0, 1, 2, or 3, the operation start timing is delayed for 0.2 ms after DIR output changes (To prevent malfunction of a motor driver). |
| 09h | 18 to 16 | EPW | When “RENV1.CDWS = 0”, select ERC signal output pulse width.<br>When “RENV1.CDWS = 1”, select current up timer.<br>000: 12 µs 001: 102 µs 010: 409 µs 011: 1.6 ms<br>100: 13 ms 101: 52 ms 110: 104 ms 111: Level output |
| | 19 | ERCL | Select ERC/CDW signal logic.<br>0: Negative logic.<br>1: Positive logic. |
| | 22 to 20 | ETW | When “RENV1.CDWS = 0”, select ERC signal OFF timer time.<br>When “RENV1.CDWS = 1”, select current down timer.<br>000: 0 µs 001: 12 µs 010: 1.6 ms 011: 52 ms<br>101: 208 ms 100: 104 ms 110: 416 ms 111: 832 ms<br>When “RENV1.CDWS = 1” is set, the current down timer is set. |
| | 23 | CDWS | Select the output signal from ERC/CDW terminal.<br>0: ERC signal (Deviation counter clear signal).<br>1: CDW signal (current down signal). |

| Address | Bit | Name | Description |
|---|---|---|---|
| 08h | 24 | EROE | ERC signal output due to abnormal stops<br>0: Disabled.<br>1: Enabled.<br>ERC signal is output when operation is stopped immediately by EL signal input or emergency stop command input.<br>ERC signal is not output when operation decelerate and stop. |
| | 25 | EROR | ERC signal output by origin return completion<br>0: Disabled.<br>1: Enabled.<br>ERC signal is automatically output when origin return movement is completed.<br>ERC signal is output even when deceleration stop is performed. |
| | 26 | PHMK | Excitation sequence output<br>0: Enabled.<br>1: Disabled.<br>Excitation sequence is output. |
| | 27 | PHMA | Excitation sequence output is tuned OFF by CDW signal.<br>0: Disabled.<br>1: Enabled.<br>While CDW signal is output, excitation sequence output turns off. |
| | 30~28 | IDL | Set the idling signal count.<br>0: Disabled.<br>1 to 7: Enabled. The idling signal count is a setting value n − 1.<br>When high-speed patterns are used, acceleration starts after outputting idling pulses at FL speed.<br>See “10.3 Idling control” for details. |
| | 31 | MSKP | Masking function of output pulse<br>0: Disabled.<br>1: Enabled.<br>The pulse output is masked and the excitation sequence output is not changed. |

* Output pulses with RENV1.PMD bits of “000” and “101” are shown below:



# 7.12 RENV2: Environment setting 2 register

Register for Environment setting 2. [Address: 05h to 07h]

Mainly specifications for general-purpose I/O ports, encoder signal input, manual pulser signal input, and origin return movement are set.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EPSE | EECE | ESDW | ESTA | ECMD | EEND | MSKI |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STAF | PINF | PIM | | EOFF | EINF | EIM | | EZD | | | | EZL | CUNI | ORCR | ORM |

| Address | Bit | Name | Description |
|---|---|---|---|
| 07h | 0 | ORM | Select origin return movement specification.<br>0: In constant-speed patterns, operation stops immediately when ORG signal input tunes OFF to ON.<br>In high-speed patterns, deceleration stop is performed when ORG signal input turns OFF to ON (Pass through ORG).<br>1: For constant-speed patterns, immediate stop is performed by counting EZ signals after ORG signal inputs turns OFF to ON.<br>For high-speed patterns, decelerates when ORG signal input turns OFF to ON, and immediately stop by counting EZ signal. |
| | 1 | ORCR | Reset current position counter of origin return movement.<br>0: Disabled.<br>1: Enabled.<br>Resets the current position counter at the origin position in origin return movement. |
| | 2 | CUNI | Select the input of current position counter.<br>0: Output pulse.<br>1: Encoder signals (EA and EB). |
| | 3 | EZL | Select EZ-signal logic.<br>0: Negative logic (count at the falling edge).<br>1: Positive logic (count at the rising edge). |
| | 7 to 4 | EZD | Set EZ signal count value.<br>0 to 15: 1 to 16 times. Set a value “count number − 1”. |
| 06h | 9, 8 | EIM | Select the encoder signal (EA, EB) input specification.<br>00: 90-degree phase difference; 1x (count up when the phase of EA signal is advanced).<br>01: 90-degree phase difference; 2x (count up when the phase of EA signal is advanced).<br>10: 90-degree phase difference; 4x (count up when the phase of EA signal is advanced).<br>11: Counting up at the rising edge of EA signal and counting down at the rising edge of EB signal. |
| | 10 | EINF | Input noise filter for EA, EB, and EZ terminal.<br>0: Recognize a signal with a pulse width of 0.1 µs or wider.<br>1: Recognize a signal with a pulse width of 0.3 µs or wider. |
| | 11 | EOFF | EA and EB signal inputs<br>0: Enabled.<br>1: Disabled. |
| | 13, 12 | PIM | Select manual pulser signals (PA/PB) input method.<br>00: 90-degree phase difference; 1x (count up when the phase of PA signal is advanced).<br>01: 90-degree phase difference; 2x (count up when the phase of PA signal is advanced).<br>10: 90-degree phase difference; 4x (count up when the phase of PA signal is advanced).<br>11: Counting up at the rising edge of PA signal and counting down at the rising edge of PB signal. |
| | 14 | PINF | Input noise filters for PA/PDR and PB/MDR terminals.<br>0: Recognize a signal with a pulse width of 0.1 µs or wider.<br>1: PDR signal and MDR signal recognize signals with a pulse width of 40 ms or wider.<br>PA signal and PB signal recognize signals with a pulse width of 0.3 µs or wider. |
| | 15 | STAF | Input noise filters for STA and STP terminals.<br>0: Recognize a signal with a pulse width of 0.5 µs or wider.<br>1: Recognize a signal with a pulse width of 40 ms or wider.<br>Note: Select “RENV2.STAF = 0” when using STAO (12h) command. |

| Address | Bit | Name | Description |
|---|---|---|---|
| 05h | 16 | MSKI | Mask output from INT terminal<br>0: Disabled. INT signal is output.<br>1: Enabled. RIST register changes. |
| | 17 | EEND | Interrupt of normal stop by operation mode other than continuous movement<br>0: Disabled.<br>1: Enabled. |
| | 18 | ECMD | Interrupt of arbitrary stop by stop command<br>0: Disabled.<br>1: Enabled (It does not occur with EMGSP (30h) commands). |
| | 19 | ESTA | Interrupt of simultaneous start by STA signal input<br>0: Disabled.<br>1: Enabled.<br>Note: It cannot be used in stand-alone operation. |
| | 20 | ESDW | Interrupt at deceleration start<br>0: Disabled.<br>1: Enabled. |
| | 21 | EECE | Interrupt of encoder signal input error<br>0: Disabled.<br>1: Enabled.<br>Input errors occur when EA and EB signals change simultaneously in 90-degree phase difference mode or when EA and EB signals rise simultaneously in 2-pulse mode. |
| | 22 | EPSE | Interrupt of manual pulser signal input errors<br>0: Disabled.<br>1: Enabled.<br>Input errors occur when PA and PB signals change simultaneously in 90-degree phase difference mode or when PA and PB signals rise simultaneously in 2-pulse mode. |
| | 23 | - | Must always set “0”. |
| 04h | 31~24 | - | Must always set “0”. |

# 7.13 RSTS: Status information register

Register to acquire the status information. [Address: 26h to 29h]

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SINT | SSTP | SSTA | SSDP | SCM | | | | SERC | SINP | SORG | SDIN | SSD | SPEL | SMEL | SMVZ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SPA | SPB | SEA | SEB | SZC | | | | SEZ | SPFH | SPUB | SPHZ | SPH4 | SPH3 | SPH2 | SPH1 |

| Address | Bit | Name | Description |
|---|---|---|---|
| 29h | 3 to 0 | SPH4 to SPH1 | Phase signal (PH4 to PH1)<br>0: L level.<br>1: H level. |
| | 4 | SPHZ | Excitation sequence status<br>0: Other than the default.<br>1: Default. |
| | 5 | SPUB | UB terminal<br>0: L level (unipolar drive).<br>1: H level (bipolar drive). |
| | 6 | SPFH | FH terminal<br>0: L level (full step).<br>1: H level (half step). |
| | 7 | SEZ | EZ signal<br>0: OFF.<br>1: ON. |
| 28h | 11 to 8 | SZC | EZ counter value<br>Range: from “RENV2.EZD” to “0”. |
| | 12 | SEB | EB terminal<br>0: L level.<br>1: H level. |
| | 13 | SEA | EA terminal<br>0: L level.<br>1: H level. |
| | 14 | SPB | PB signal<br>0: L level.<br>1: H level.<br>It becomes “0” with operation mode of switch control (“RMD.MOD = 7h” and “RMD.MOD = 8h”). |
| | 15 | SPA | PA signal<br>0: L level.<br>1: H level.<br>It becomes “0” with operation mode of switch control (“RMD.MOD = 7h” and “RMD.MOD = 8h”). |

| Address | Bit | Name | Description |
|---|---|---|---|
| 27h | 16 | SMVZ | Counter value of remaining pulse number<br>0: Other than 0.<br>1: 0. |
| | 17 | SMEL | MEL signal<br>0: OFF.<br>1: ON. |
| | 18 | SPEL | PEL signal<br>0: OFF<br>1: ON |
| | 19 | SSD | SD Latch signal<br>0: OFF.<br>1: ON. |
| | 20 | SDIN | SD signal<br>0: OFF.<br>1: ON. |
| | 21 | SORG | ORG signal<br>0: OFF.<br>1: ON. |
| | 22 | SINP | INP signal<br>0: OFF.<br>1: ON. |
| | 23 | SERC | ERC/CDW signal<br>0: OFF.<br>1: ON. |
| 26h | 27~24 | SCM | Operation status monitor<br>0000: Being stopped<br>0001: Preparing switch control<br>0010: STA signal input waiting<br>0011: Manual pulser signal input waiting<br>0100: Direction change timer waiting<br>0101: ERC signal OFF timer waiting<br>0110: Current up timer waiting<br>0111: In constant-speed (FL speed)<br>1000: Under acceleration<br>1001: In constant-speed (FH1 speed)<br>1010: In constant-speed (FH2 speed)<br>1011: Under deceleration<br>1100: INP signal input waiting<br>1111: Start / stop processing in progress |
| | 28 | SSDP | Slow-down point passage<br>0: Before the point.<br>1: After the point. |
| | 29 | SSTA | STA terminal<br>0: H level (OFF).<br>1: L level (ON). |
| | 30 | SSTP | STP signal<br>0: OFF.<br>1: ON. |
| | 31 | SINT | INT terminal<br>0: H level (OFF).<br>1: L level (ON). |

# 7.14 RIST: Interrupt factor reset register

Register to check and reset interrupt factors. [Address: 2Ah to 2Bh]
Target bit can be reset by writing “1” to the bit to reset.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | ISDW | ISTA | ICMD | IEND | IPSE | IECE | IPOV | ISSD | ISTP | IPEL | IMEL |

| Address | Bit | Name | Description |
|---|---|---|---|
| 2Bh | 0 | IMEL | 1: Stopped by MEL signal input. |
| | 1 | IPEL | 1: Stopped by PEL signal input. |
| | 2 | ISTP | 1: Stopped by STP signal input. |
| | 3 | ISSD | 1: Stopped by SD signal input turned ON. |
| | 4 | IPOV | 1: Manual pulser signal input overflows. |
| | 5 | IECE | 1: Encoder signal input error occurs (does not stop). *1 |
| | 6 | IPSE | 1: Manual pulser signal input error occurs (does not stop). *1, *2 |
| | 7 | IEND | 1: Normal stop by operation mode other than continuous movement. *1 |
| 2Ah | 8 | ICMD | 1: Intentional stop by commands (STOP, SDSTP). *1 |
| | 9 | ISTA | 1: When “RSTS.SCM = 0010”, STA = L level. *1<br>When “RENV1.STAM = 1” and “STA = L” are set, the operation does not start even if a start command is written. Since the interrupt condition is satisfied, it becomes “RIST.ISTA = 1”. |
| | 10 | ISDW | 1: Deceleration starts *1 |
| | 11 | - | Always “0”. |
| | 12 | - | Always “0”. |
| | 13 | - | Always “0”. |
| | 14 | - | Always “0”. |
| | 15 | - | Always “0”. |

*1: To generate this interrupt, you must allow interrupt occurrence by RENV2 register.

| Interrupt flag | Target bit |
|---|---|
| RIST.IECE (5) | RENV2.EECE (21) bit |
| RIST.IPSE (6) | RENV2.EPSE (22) bit |
| RIST.IEND (7) | RENV2.EEND (17) bit |
| RIST.ICMD (8) | RENV2.ECMD (18) bit |
| RIST.ISTA (9) | RENV2.ESTA (19) bit |
| RIST.ISDW (10) | RENV2.ESDW (20) bit |

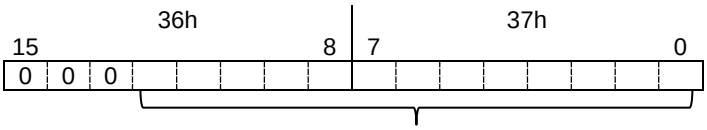
*2: “RIST.IPSE = 1” may occur when setting switch control operation mode (RMD.MOD = 7h and RMD.MOD = 8h).
In this case, set “RENV2.EPSE = 0” before changing RMD register.

When interrupt occurs, “L level” INT signal is output from INT terminal.
INT signal output can be masked by “RENV2.MSKI = 1”.
Even if INT-signal output is masked, RIST register changes with interrupt.

Note: When the upper byte that has been set with an interrupt factor is reset, INT signal becomes “H level”.
At this time, if the interrupt factor has also been set in the lower byte, INT signal returns to “L level”.
INT signal changes in the same manner even if the lower byte is reset first.
Note that INT signal changes per byte when the upper byte and the lower byte are reset by one writing operation.

## 7.15 RSPD: Current speed reading register

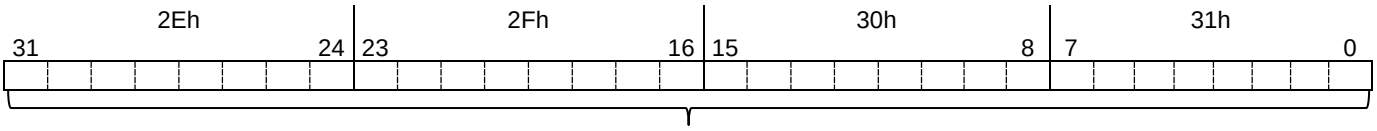
Current speed can be read by speed step value. [Address: 36h to 37h]
It is “0” when stopped.




Current speed step value: 0 to 8,191

## 7.16 RCUN: Current position register

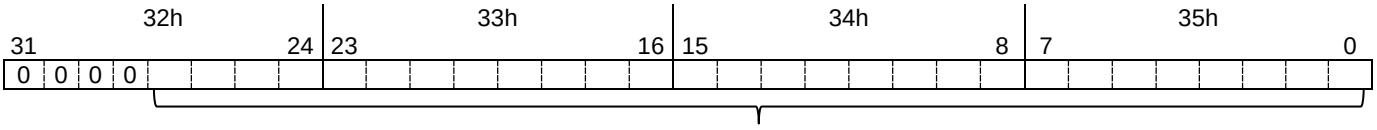
It is the current position counter. [Address: 2Eh to 31h]
A negative number is shown in 2's complement.




Current position : −2,147,483,648 to +2,147,483,647

## 7.17 RDWC: Remaining-pulse number reading register

Remaining-pulse number can be read by incremental movement such as positioning control. [Address: 32h to 35h]




Number of pulse: 0 to 268,435,455

# 7.18 RIOP: General-purpose I/O port configuration register

I/O can be selected for general-purpose I/O terminals (P0, P1) during CPU-connected system (MODE = L).

[Address: 2CH to 2Dh]

It is also possible to change the output and to check the status of the general-purpose I/O terminals (P0, P1) set for general-purpose output and general-purpose output terminals (P2, P3).

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | PMD1 | PMD0 | 0 | 0 | 0 | 0 | PDT3 | PDT2 | PDT1 | PDT0 |

| Address | Bit | Name | Description |
|---|---|---|---|
| 2Dh | 0 | PDT0 | Writing is the state of P0 output data and reading is the state of P0 terminal.<br>0: L level<br>1: H level |
| | 1 | PDT1 | Writing is the state of P1 output data and reading is the state of P1 terminal.<br>0: L level<br>1: H level |
| | 2 | PDT2 | Writing is the state of P2 output data and reading is the state of P2 terminal.<br>0: L level<br>1: H level |
| | 3 | PDT3 | Writing is the state of P3 output data and reading is the state of P3 terminal.<br>0: L level<br>1: H level |
| | 4 to 7 | - | Must always set “0”. |
| 2Ch | 8 | PMD0 | P0 terminal selection<br>0: General-purpose input<br>1: General-purpose output |
| | 9 | PMD1 | P1 terminal selection<br>0: General-purpose input<br>1: General-purpose output |
| | 10~15 | - | Must always set “0”. |

The usability of general-purpose I/O terminals and general-purpose output terminals can change by system mode (MODE and MTYP state).

All general-purpose I/O terminals and general-purpose output terminals cannot be used in a stand-alone operation in which CPU is not used.

# 8. Operation mode

Operation mode is set by RMD.MOD bit.

## 8.1 Command control: Continuous movement

Set “RMD.MOD = 0000b” when you use command control continuous movement for operation mode.

When a start command is written, an operation starts.
When a stop command is written, the operation stops.

The moving direction is specified by RMD.MDIR bit.

Tuning ON the EL signal ON in the moving direction will stop and end the operation.
When the moving direction is positive, PEL signal is enabled.
When the moving direction is negative, MEL signal is enabled.
When starting in reverse direction after stopped by turning ON the EL signal, it is necessary to rewrite a start command.

## 8.2 Origin signal control: Origin return

Set “RMD.MOD = 0001b” to use origin return in origin signal control for an operation mode.

When a start command is written, an operation starts.
When an ORG signal or an EZ signal is input, the operation stops and ends.

The motion direction can be specified by RMD. MDIR bit.

The stopping method by signal inputs can be specified by RENV2.ORM.bit.
If you select “RENV2.ORM = 1” (stopped by EZ count), set the number to count in RENV2.EZD. “RENV2.EZD + 1” will be counted.
When “0” is set, EZ signal is counted once.

ERC signal can be output when origin return movement is completed.
See “7.11 RENV1: Environment setting 1 register” for details.

## 8.3 Origin return with feeding amount limit

Set “RMD.MOD=0010b” when using origin return with feeding amount limit for operation mode.

When a start command is written, an operation starts.
After starting, RMV register value is copied to RDWC register and counted down for each pulse output.
When ORG signal or EZ signal is input, or it becomes “RDWC = 0”, the operation stops and ends.

The moving direction is specified by RMD.MDIR bit.

RSTS.SMVZ bits allow you to determine whether you stopped at the origin or by feeding amount limit.
“RSTS.SMVZ = 0” indicates “stopped at origin position”, and “RSTS.SMVZ = 1” indicates “stopped by feeding amount limit”.

The stopping method by signal inputs can be specified by RENV2.ORM bit.
If you select “RENV2.ORM = 1” (stopped by EZ count), set the number to count to RENV2.EZD.
“RENV2. EZD +1” will be counted.
If “0” is set, EZ signal is counted once.

ERC signal can be output when origin return to origin operation is completed.
See “7.11 RENV1: Environment setting 1 register” for details.

## 8.4 Origin signal control: Origin escape operation

Set “RMD.MOD=0011b” when using origin escape operation in origin signal control for operation mode.

When a start command is written, an operation starts.
When an ORG signal turns OFF, the operation stops and ends.

The moving direction is specified by RMD. MDIR bit.

For the start command, use constant-speed start (STAFL (40h), STAFH1 (41h), and STAFH2 (42h) commands).

When a start command is written while ORG signal is OFF, the operation stops without outputting pulses.

ORG signal samples during outputting pulses.
When an operation starts while ORG signal is ON, only one pulse is output after ORG signal is turned OFF, and then the operation stops.

## 8.5 EL signal (End Limit signal) control: EL escape operation

Set “RMD.MOD=0100b” when using EL escape operation in EL signal control for operation mode.

When a start command is written, an operation starts.
When EL signal in the opposite to moving direction is turned OFF, an operation stops and ends.

The motion direction is specified by RMD. MDIR bit.

For start commands, use constant-speed start (STAFL (40h), STAFH1 (41h), and STAFH2 (42h) commands).

If an EL signal in the opposite to the moving direction is OFF and a start command is written, the operation stops without outputting pulses.

## 8.6 Positioning control: Incremental movement

Set “RMD.MOD=0101b” when using incremental movement of the positioning control for operation mode.

When a start command is written, an operation starts.
When starting, RMV register value is copied to RDWC register and count down at every pulse output.
When “RDWC = 0”, the operation stops and ends.

The motion direction is specified by RMD.MDIR bits.

## 8.7 Positioning control: Timer

To use the positioning control operation time as a timer, set “RMD.MOD = 0110b”.

When a start command is written, operation starts.
RMV register value is copied to RDWC register after starting and count down at every pulse output.
When “RDWC = 0”, the operation stops and ends.

No pulse is output.
The timer time is calculated from the output pulse cycle and the RMV register value.

Input of EL signal, SD signal and INP signals are disabled.
STP signal input can be enabled.
The direction change timer is disabled.
The counting of the RCUN register is also disabled.

# 8.8 Switch control: Continuous movement

Set “RMD.MOD = 0111b” when using switch control continuous movement for operation mode.

After writing a start command, it becomes “RSTS.SCM = 1111b”.
At this time, while drive switch signal (PDR signal or MDR signal) is ON, continuous movement is performed.
When STOP (31h) command is written, operation mode ends.

The drive switch signal is an edge trigger.
Even if the start command is written with the drive switch signal ON, it will not operate.

When PDR signal turns ON, it moves in the positive direction, and when it is OFF, the operation stops.
When MDR signal is already ON, the PDR signal ON input is ignored.
When MDR signal turns ON, it moves in the negative direction and stops when it is OFF.
When PDR signal is already ON, MDR signal ON input is ignored.
RMD.MDIR bit is disabled.

When the speed is in high-speed pattern, deceleration stop is performed by turning OFF drive switch signal.
When driving switch signal ON in opposite direction is input while decelerating by the input of drive switch signal OFF, the movement reverses after deceleration stop.

If EL signal in the moving direction turns ON, the operation stops.
Interrupt does not occur when EL signal turns on.
When motion starts in reverse direction after being stopped by EL signal turning ON, it is unnecessary to rewrite a start command.

# 8.9 Switch control: Incremental movement

Set RMD.MOD = 1000b when using incremental movement in switch control motion for operation mode.

After writing a start command, it becomes “RSTS.SCM = 1111b”.
Each time the drive switch signal (PDR signal or MDR signal) changes from OFF to ON, an incremental movement is performed.
After starting, RMV register value is copied to RDWC register and counted down at every pulse output.
When “RDWC = 0”, operation stops.
When STOP (31h) command is written, operation mode ends.

The moving direction is in positive by PDR signal input and in negative by MDR signal input.
Simultaneous input of PDR signal and MDR signal is ignored.
The additional input during running is also ignored.
Setting of RMD.MDIR bit is enabled.

Operations stop when EL signal in the moving direction turns ON.
Interrupt does not occur when EL signal turns ON.
If the movement starts in reverse direction after being stopped by EL signal turning ON, it is unnecessary to rewrite a start command.

When stop by EL signal, interrupt of normal stop (RIST.IEND) by operation mode other than continuous movement does not occur. I will not be “RDWC = 0”, and the count value in the middle is maintained.
RSTS.SMVZ bit also does not become “1”.
Please judge stop by EL signal from these conditions.

When “0” is set in RMV register, no pulse is output, but the direction signal changes.

When “DIR = H level” with “RENV1.PMD = 000b”, if writing a start command with “RMD.DIR = 0”, it will be “DIR = H level”.
When “DIR = H level” with “RENV1.PMD = 000b”, if writing a start command with “RMD.DIR = 1”, it will be “DIR = L level”.

# 8.10 Pulser control: Continuous movement

Set RMD.MOD = 1001b when using pulser control continuous movement for operation mode.

When a start command is written, “RSTS.SCM = 0011b” while BSY signal is OFF.
When manual pulser signals (PA signal and PB signal) are input, BSY signal turns ON and pulse signals are output.
When STOP (31h) command is written, operation mode ends.

Moving direction is the same as input direction of manual pulser signals.

For start commands, use constant-speed start (STAFL (40h), STAFH1 (41h), or STAFH2 (42h) commands).

When EL signal in the moving direction is input, the operation will be as follows.

1. It stops to output pulse.
2. INT signal does not output.
3. Operation mode does not end.

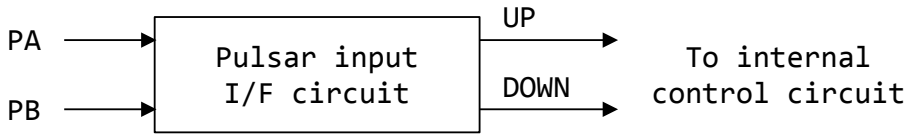
When the input of pulser signal is reversed while EL signal is being input, the number of output pulses will be less than the number of input pulses.

When the manual pulsar signal exceeds the maximum input frequency (FP), the input buffer counter (signed 8 bit) overflows. Please use FP within the following range.

$$\mathrm{FP[pps]} < \frac{\text{FH Speed [pps]}}{\text{Input I/F multipliplication value}}$$

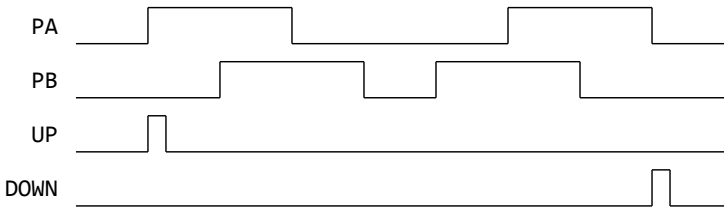
| Manual pulser signal input specification | Input I/F multipliplication value |
|---|---|
| 90-degree phase difference; 1x | 1 |
| 90-degree phase difference; 2x | 2 |
| 90-degree phase difference; 4x | 4 |
| 2-pulse signal | 1 |

When the input buffer counter overflows, an interrupt (REST.IPOV) is generated.

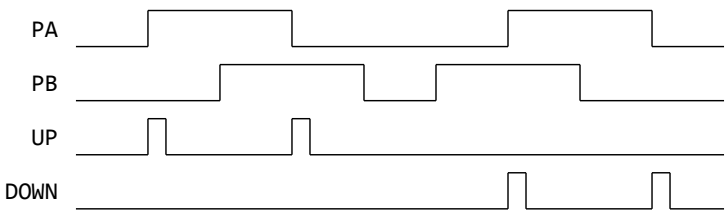



RENV2.PIM bit can be used to select the input specifications of manual pulser signal.

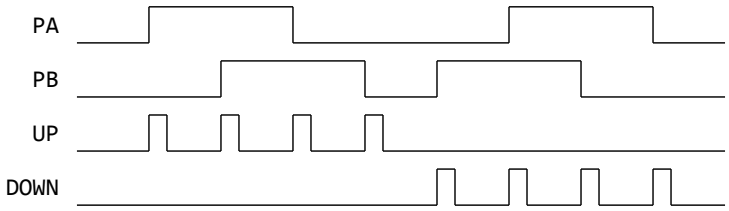
1) 90-degree phase difference signal 1x input (RENV2. PIM = 00)



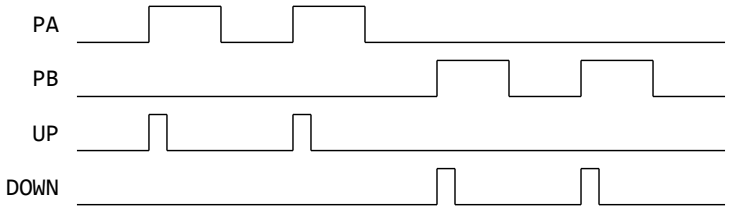

2) 90-degree phase difference signal 2x input (RENV2.PIM = 01)



3) 90-degree phase difference signal 4x input (RENV2.PIM = 10)




4) 2-pulse signal input (RENV2.PIM = 11)




# 8.11 Pulser control: Incremental movement

Set “RMD.MOD = 1010b” when using incremental movement in pulser control.

When a start command is written, “RSTS.SCM=0011b” while BSY signal is OFF.
After starting, RMV register value is copied to RDWC register and counted down at every pulse output.
When a manual pulser signal (PA signal, PB signal) is input, BSY signal turns ON and pulse is output.
When “RDWC = 0”, the operation stops, and the operation mode ends.
After ending the operation mode, input of manual pulser signal is ignored.

The moving direction is specified by RMD.MDIR bits.
It is not the same as the direction of manual pulser signals.

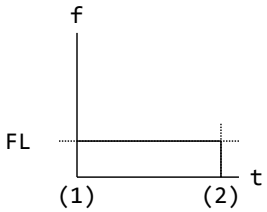
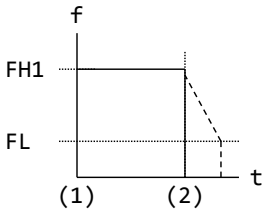
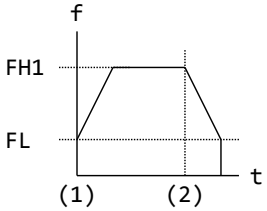
For start commands, use constant-speed start (STAFL (40h), STAFH1 (41h), and STAFH2 (42h) commands).

Stops when EL signal in the operation direction turns ON.
Interrupt occurs when EL signal is turned on.
Start command must be rewritten to start backward after stopping by EL turned on.
When motion starts in reverse direction after being stopped by EL signal turning ON, it is necessary to rewrite a start command.

If “0” is set in RMV register, the operation mode ends immediately after a start command is written.

# 9. Speed pattern

## 9.1 Speed pattern list

| Speed pattern | Continuous movement operation mode | Incremental movement operation mode |
|---|---|---|
| FL constant-speed patterns<br>  <br> | (1) Writing STAFL (40h) command<br>(2) Stopped by writing STOP (31h) command<br><br>* Operations can also immediately stop when writing SDSTP (32h) command. | (1) Writing STAFL(40h) command<br>(2) Stopped by “RDWC = 0” or STOP (31h) commands.<br><br>* Operations can also immediate stop by SDSTP (32h) commands. |
| FH1 constant-speed patterns<br>※The same applies to FH2 constant-speed pattern.<br>  <br> | (1) Writing STAFH1 (41h) command<br>(2) Stopped by writing STOP (31h) command<br><br>* Deceleration starts when writing SDSTP (32h) command. | (1) Writing STAFH1(41h) command<br>(2) Stopped by writing “RDWC = 0” or STOP (31h) command.<br><br>* Deceleration starts when writing SDSTP (32h) command. |
| FH1 fast pattern<br>※ The same applies to FH2 high-speed pattern.<br>  <br> | (1) Writing STAUD1 (43h) command<br>(2) Deceleration starts by writing SDSTP (32h) command.<br><br>* Operations can immediately stop when writing STOP (31h) command. | (1) Writing STAUD1(43h) command<br>(2) Deceleration starts by reaching slow-down point or writing SDSTP (32h) command.<br><br>* Operations can immediately stop by writing STOP (31h) command.<br><br>* When setting “RMD.MSDP = 1” (slow-down point manual setting) and “RDP = 0” (without slow-down point) at the same time, the movement stops immediately. |

# 9.2 Speed pattern setting

The speed pattern is set in the registers shown in the table below.
If the value to be set is the same as the previous value, no need to written again.
Please note that “0” is out of the setting range in some registers.

| Register | Content | Bit-length | Setting range | R/W |
|---|---|---|---|---|
| RMV | Number of output pulse | 28 | 0 to 268,435,455 (FFFFFFFh) | R/W |
| RFL | Starting speed | 13 | 1 to 8,191 (1FFFh) | R/W |
| RFH | Operation speed | 13 | 1 to 8,191 (1FFFh) | R/W |
| RUR | Acceleration rate | 16 | 1 to 65,535 (FFFFh) | R/W |
| RDR | Deceleration rate * | 16 | 1 to 65,535 (FFFFh) | R/W |
| RMG | Speed magnification | 12 | 3 to 4,095 (FFFh) | R/W |
| RDP | Slow-down point | 24 | −8,388,608 (800000h) to +8,388,607 (7FFFFFh)<br>0 to 16,777,215 (FFFFFFh) | R/W |
| RUS | Acceleration S-curve section | 12 | 0 to 4,095 (FFFh) | R/W |
| RDS | Deceleration S-curve section | 12 | 0 to 4,095 (FFFh) | R/W |

* When “RDR = 0” is set, deceleration rate becomes RUR register value.

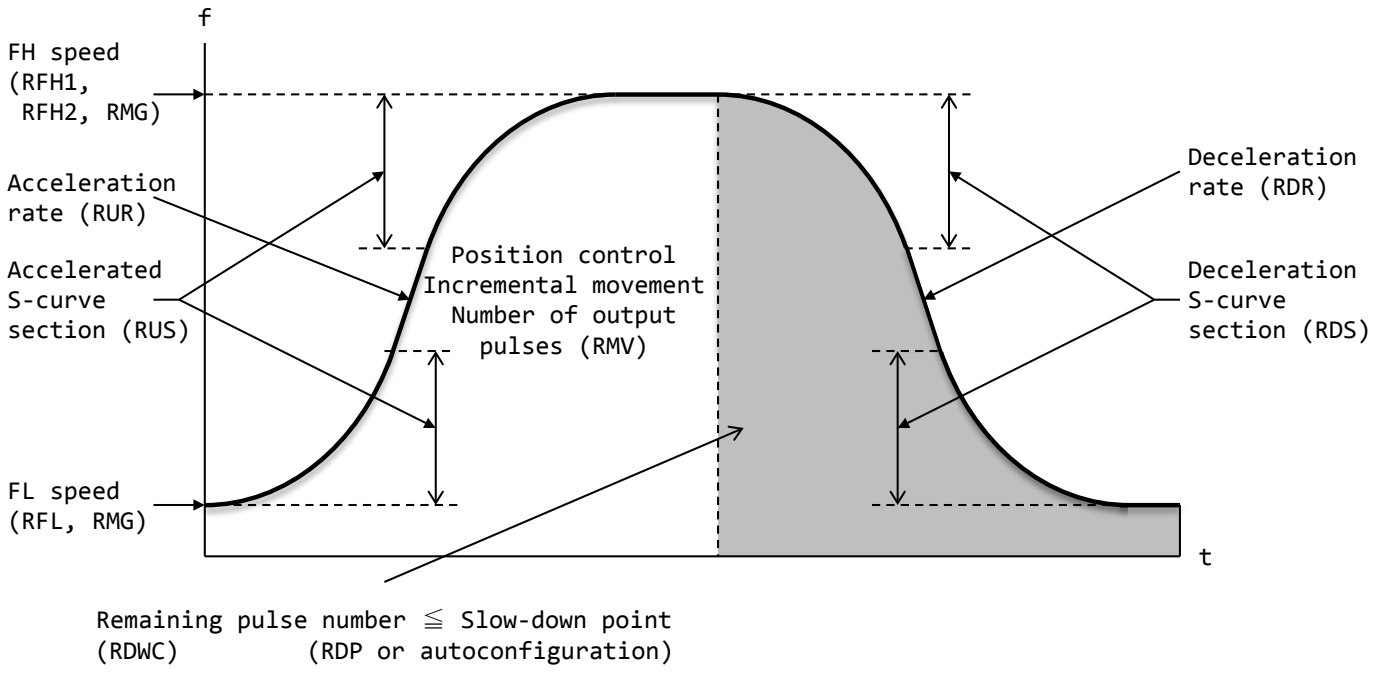



**Fig. 9.2-1 High-speed pattern register setting**

Note: CLK [Hz] used in the following equations is the frequency [Hz] of CLK signal

## 9.2.1 RMV: Number of output pulses setting register (28 bits)

Register to set the number of pulses to be output (=feeding amount) by the operation mode of incremental movement.
The setting range is from 0 to 268,435,455 (0FFF FFFFh).

## 9.2.2 RFL: FL speed setting register (13 bits)

Register to set the FL speed (initial speed, stopping speed) in FL constant-speed pattern or FH high-speed pattern by speed step value.
The setting range is from 1 to 8,191 (1FFFh).
The actual speed is the calculated value with RMG register value.

$$FL[pps] = RFL \times \frac{CLK[Hz]}{(RMG+1)\times 8{,}192} \qquad RFL = FL[pps] \times \frac{(RMG+1)\times 8{,}192}{CLK[Hz]}$$

$$= RFL\ x\ MG$$

FL: FL speed
MG: Speed magnification

For speed magnification, see “9.2.6 RMG: Speed magnification setting register (12 bits)”.

## 9.2.3 RFH: FH speed setting register (13 bits)

Register to set the FH constant-speed pattern or FH speed (operation speed) for high-speed pattern using speed step value.
The setting range is from 1 to 8,191 (1FFFh).
The actual speed is the calculated value with RMG register value.
For FH high-speed patterns, set a value larger than RFL register value.

Speed override can be used with speed change commands of RFH register different from active RFH register.
When the current speed is FH1 speed, you can change to FH2 speed by writing the speed change command FSCHH2 (65h) to FH2 speed during operation.
In serial communication, register values are changed in units of byte.
If you directly change FH register value while operation at FH speed, the time difference may result in unintended register values.
See “9.5 Target speed override” for details.

$$FH1[pps] = RFH1 \times \frac{CLK[Hz]}{(RMG+1)\times 8{,}192} \qquad RFH1 = FH1[pps] \times \frac{(RMG+1)\times 8{,}192}{CLK[Hz]}$$

$$= RFH\ 1x\ MG$$

FH1: FH1 speed
MG: Speed magnification

$$FH2[pps] = RFH2 \times \frac{CLK[Hz]}{(RMG+1)\times 8{,}192} \qquad RFH2 = FH2[pps] \times \frac{(RMG+1)\times 8{,}192}{CLK[Hz]}$$

$$= RFH2x\ MG$$

FH2: FH2 speed
MG: Speed magnification

For speed magnification, see “9.2.6 RMG: Speed magnification setting register (12 bits)”.

## 9.2.4 RUR: Acceleration rate setting register (16 bits)

Register to set acceleration rate.
The setting range is from 1 to 65,535 (FFFFh).
The relationship between the set value and the acceleration time is as follows.

1) Linear acceleration (RMD.MSMD = 0)

$$TU[s] = \frac{(RFH - RFL) \times (RUR + 1) \times 2}{CLK[Hz]} \qquad RUR = \frac{CLK[Hz] \times TU[s]}{(RFH - RFL) \times 2} - 1$$

TU: Acceleration time [s]

2) S-curve acceleration without linear range (RMD.MSMD = 1 and RUS = 0)

$$TU[s] = \frac{(RFH - RFL) \times (RUR + 1) \times 4}{CLK[Hz]} \qquad RUR = \frac{CLK[Hz] \times TU[s]}{(RFH - RFL) \times 4} - 1$$

TU: Acceleration time [s]

3) S-curve acceleration with linear range (RMD.MSMD = 1 and RUS > 0)

$$TU[s] = \frac{(RFH - RFL + 2 \times RUS) \times (RUR + 1) \times 2}{CLK[Hz]} \qquad RUR = \frac{CLK[Hz] \times TU[s]}{(RFH - RFL + 2 \times RUS) \times 2} - 1$$

TU: Acceleration time [s]

## 9.2.5 RDR: Deceleration rate setting register (16 bits)

Register to set deceleration rate.
The setting range is from 0 to 65,535 (FFFFh).
When “RMD.MSDP = 0” (slow-down point (=ramping-down point) is automatically set, set the same as RUR register value or set “RDR = 0”.
When “RDR=0” is set, deceleration rate is the same as RUR register.
The relationship between the set value and the deceleration time is as follows.

1) Linear deceleration (RMD.MSMD = 0)

$$TD[s] = \frac{(RFH - RFL) \times (RDR + 1) \times 2}{CLK[Hz]} \qquad RDR = \frac{CLK[Hz] \times TD[s]}{(RFH - RFL) \times 2} - 1$$

TD: Deceleration time [s]

2) S-curve deceleration without linear section (RMD.MSMD = 1 and RDS = 0)

$$TD[s] = \frac{(RFH - RFL + 0.25) \times (RDR + 1) \times 4}{CLK[Hz]} \qquad RDR = \frac{CLK[Hz] \times TD[s]}{(RFH - RFL + 0.25) \times 4} - 1$$

TD: Deceleration time [s]

3) S-curve deceleration with linear section (RMD.MSMD = 1 and RDS > 0)

$$TD[s] = \frac{(RFH - RFL + 2 \times RDS + 0.5) \times (RDR + 1) \times 2}{CLK[Hz]} \qquad RDR = \frac{CLK[Hz] \times TD[s]}{(RFH - RFL + 2 \times RDS + 0.5) \times 2} - 1$$

TD: Deceleration time [s]

## 9.2.6 RMG: Speed magnification setting register (12 bits)

Register to set speed magnification.
The setting range is from 3 to 4,095 (0FFFh).
It sets the relationship between RFL register value / RFH register value and the actual speed [pps].
The actual speed is the product of speed magnification and speed register value.
The higher the magnification, the coarser / wider the speed interval becomes.
Usually, use as low a magnification as possible.
The relationship between setting values and speed magnifications is as follows:

$$MG = \frac{CLK[Hz]}{(RMG + 1) \times 8{,}192} \qquad RMG = \frac{CLK[Hz]}{MG \times 8{,}192} - 1$$

MG: speed magnification

When the reference clock frequency is 9.8304 MHz, the speed magnification will be shown in the table below:

| Setting value | Speed magnification (MG) | Output speed range (pps) | | |
|---|---|---|---|---|
| 2399 (95Fh) | 0.5 | 0.5 | to | 4,095.5 |
| 1199 (4AFh) | 1 | 1 | to | 8,191 |
| 599 (257h) | 2 | 2 | to | 16,382 |
| 239 (0EFh) | 5 | 5 | to | 40,955 |
| 119 (077h) | 10 | 0 | to | 81,910 |

| Setting value | Speed magnification (MG) | Output speed range (pps) | | |
|---|---|---|---|---|
| 59 (03Bh) | 20 | 20 | to | 163,820 |
| 23 (017h) | 50 | 50 | to | 409,550 |
| 11 (00Bh) | 100 | 100 | to | 819,100 |
| 5 (005h) | 200 | 200 | to | 1,638,200 |
| 3 (003h) | 300 | 300 | to | 2,457,300 |

## 9.2.7 RDP: Slow-down point setting register (24 bits)

Register to set slow-down point (= ramping-down point: number of remaining pulse to start deceleration) used for positioning control and so on. It is used when operation mode is incremental movement and speed pattern is high-speed pattern.

When the value of slowdown point is larger than the optimum value, deceleration starts early. Also the number of pulses operating at FL speed increases, so the stop is delayed.
If the value is smaller than the optimum value, deceleration starts late and the stopping speed becomes faster than FL speed, so it will stop earlier.

<Manual setting> (RMD.MSDP = 1)

Set the number of pulse in slow-down point:
The setting range is from 0 to 16,777,215 (FFFFFFh).

Deceleration starts when number of remaining pulses is equal to or less than RDP register value.

Note: To find an appropriate RDP register value for manual setting, you must know the actual maximum speed.
If deceleration occurs during acceleration, or operation speed is changed by “RMD.MADJ = 0”, manual setting value cannot be calculated.
Set “RMD.MADJ = 1” and conduct the following calculation with the maximum speed after manual FH correction calculation.

The optimal value for slow-down point can be calculated by the following formula:

1) Linear deceleration (RMD.MSMD = 0)

$$SDP[pulse] = \frac{(RFH + RFL - 0.5) \times (RFH - RFL) \times (RDR + 1)}{(RMG + 1) \times 8{,}192}$$

SDP: slow-down point [pulse]

2) S-curve deceleration without linear section (RMD.MSMD = 1 and RDS = 0)

$$SDP[pulse] = \frac{(RFH + RFL) \times (RFH - RFL + 0.25) \times (RDR + 1) \times 2}{(RMG + 1) \times 8{,}192}$$

SDP: slow-down point [pulse]

3) S-curve deceleration with linear section (RMD.MSMD = 1 and RDS>0)

$$SDP[pulse] = \frac{(RFH + RFL) \times (RFH - RFL + 2 \times RDS + 0.5) \times (RDR + 1)}{(RMG + 1) \times 8{,}192}$$

SDP: slow-down point [pulse]

<Auto-setting > (RMD.MSDP = 0)

Offsets to the automatically set slow-down point:
The setting range is from −8,388,608 (80 0000h) to +8,388,607 (7F FFFFh).

When the offset is a positive number, deceleration starts earlier than auto-setting value.
When it is a negative number, deceleration starts later than auto-setting value.
Set to “0” when no offset is required.

Note: Use “RMD. MSDP = 1” when the number of pulse required for acceleration and the offset calculation result are out of 24-bit range.

## 9.2.8 RUS: Acceleration S-curve section setting register (12 bits)

Register to set S-curve section in S-curve acceleration operation:
The setting range is from 1 to 4,095 (0FFFh).

$S_{SU}$ of S-curve acceleration section is calculated with RMG register value.

$$S_{SU}[pps] = RUS \times \frac{CLK[Hz]}{(RMG+1)\times 8{,}192} = RUS\,x\,MG$$

$$RUS = S_{SU}[pps] \times \frac{(RMG+1)\times 8{,}192}{CLK[Hz]}$$

$S_{SU}$: Scope of S-curve acceleration section [pps]
MG: Speed magnification

S-curve acceleration operation is performed from FL speed to (FL speed + $S_{SU}$) and from (FH speed − $S_{SU}$) to FH speed.
The intermediate section from (FL speed +$S_{SU}$) to (FH speed − $S_{SU}$) is linear acceleration.

When “0” is set, S-curve acceleration section without linear acceleration is performed by substituting $\frac{RFH-RFL}{2}$.
When the minimum value “1” is set, the operation is almost the same as linear acceleration.

Set a RUS register value that is equal to or smaller than $\frac{RFH-RFL}{2}$.

## 9.2.9 RDS: Deceleration S-curve section setting register (12 bits)

Register to set S-curve section of S-curve deceleration operation.
The setting range is from 1 to 4,095 (0FFFh).

$S_{SD}$ of S-curve deceleration section is calculated with RMG register value.

$$S_{SD}[pps] = RDS \times \frac{CLK[Hz]}{(RMG+1)\times 8{,}192} = RDS\,x\,MG$$

$$RDS = S_{SD}[pps] \times \frac{(RMG+1)\times 8{,}192}{CLK[Hz]}$$

$S_{SD}$: Scope of S-curve deceleration section [pps]
MG: Speed magnification

S-curve deceleration operation is performed from FH speed to (*FH speed* − $S_{SD}$) and from (*FL speed* + $S_{SD}$) to FL speed.
The intermediate section from (*FH speed* − $S_{SD}$) to (*FL speed* + $S_{SD}$) is linear deceleration.

When “0” is set, S-curve deceleration section without linear deceleration is performed by substituting $\frac{RFH-RFL}{2}$
When the minimum value “1” is set, the operation is almost the same as linear deceleration operation.

Set a RDS register value that is equal to or smaller than $\frac{RFH-RFL}{2}$

# 9.3 Manual FH correction calculation

Speed patterns may become a triangle profile when acceleration/deceleration is performed with incremental operation.
When FH speed is too fast to number of output pulses, or when number of output pulses is too small for the FH speed, triangle driving is used.

When “RMD.MADJ = 0” (avoid triangle driving), FH speed is automatically reduced to avoid triangle driving.
When slow-down point setting is “RMD.MSDP = 0” (slow-down auto-setting), slow-down point is also corrected.

See “9.2.7 RDP: Slow-down point setting register (24 bits)” for details.

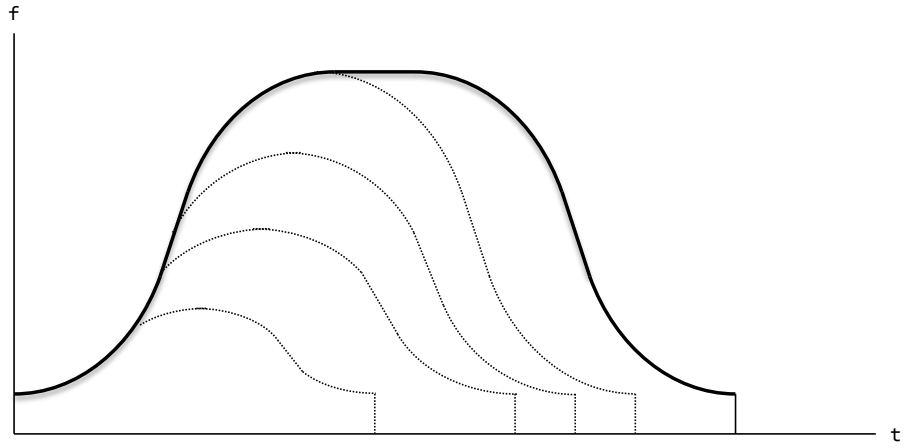



**Fig. 9.3-1 Automatic Correction of Maximum Speed by Number of Output Pulses**

“RMD.MSDP=0” can be used when acceleration and deceleration curves are symmetrical.
If acceleration and deceleration curves are asymmetric, select “RMD.MSDP = 1” (manually set for slow-down point).

When using “RMD.MSDP = 1”, use “RMD.MADJ = 1” (do not avoid triangle driving).
FH speed to avoid triangle driving is obtained by manual FH correction calculation.

Note: The speed curve when “RMD.MADJ = 1” is different from the speed curve when “RMD.MADJ = 0”.
In “RMD.MADJ = 0”, the maximum acceleration set in the RUR register and RDR register may not be reached.

## 9.3.1 Linear acceleration/deceleration

FH speed of linear acceleration/deceleration (“RMD.MSMD = 0”) can be calculated by the following equation:

$$RMV \leqq \frac{(RFH^2 - RFL^2) \times (RUR + RDR + 2)}{(RMG + 1) \times 8{,}192} \quad \text{At}$$

$$RFH \leqq \sqrt{\frac{(RMG + 1) \times 8{,}192 \times RMV}{RUR + RDR + 2} + RFL^2}$$

## 9.3.2 S-curve acceleration/deceleration without linear accel/decel section

Calculate the FH speed of S-curve acceleration/deceleration (“RUS = 0” and “RDS = 0” and “RMD.MSMD = 1”) without linear acceleration and no linear deceleration section by the following equation:

$$RMV \leqq \frac{(RFH^2 - RFL^2) \times (RUR + RDR + 2) \times 2}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

$$RFH \leqq \sqrt{\frac{(RMG + 1) \times 8{,}192 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

## 9.3.3 S-curve acceleration/deceleration with linear accel/decal section

FH speed of S-curve accel/decel where there is a linear acceleration section or a linear deceleration section (("RUS > 0" or "RDS > 0") and "RMD.MSMD = 1") is obtained by following calculation formula respectively according to relation between RUS register and RDS register.

1. When RUS = RDS
   (i) Reduce linear accel/decel sections

$$RMV \leqq \frac{(RFH + RFL) \times (RFH - RFL + 2 \times RUS) \times (RUR + RDR + 2)}{(RMG + 1) \times 8{,}192} \quad \text{and}$$

$$RMV > \frac{(\mathrm{RUS} + RFL) \times RUS \times (RUR + RDR + 2) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

$$RFH \leqq -RUS + \sqrt{(RUS + RFL)^2 + \frac{(RMG + 1) \times 8{,}192 \times RMV}{RUR + RDR + 2}}$$

   (ii) Eliminate linear accel/decel sections

$$RMV \leqq \frac{(\mathrm{RUS} + RFL) \times RUS \times (RUR + RDR + 2) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

   Change to S-curve accel/decel (RUS = 0, RDS = 0) without linear accel/decel section.

$$RFH \leqq \sqrt{\frac{(RMG + 1) \times 8{,}192 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

2. When RUS < RDS
   (i) Reduce linear accel/decel sections.

$$RMV \leqq \frac{(RFH + RFL) \times \big((RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)\big)}{(RMG + 1) \times 8{,}192} \quad \text{and}$$

$$RMV > \frac{(RDS + RFL) \times \big(RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)\big) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

$$RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$$

   However

$$A = RUS \times (RUR + 1) + RDS \times (RDR + 1)$$
$$B = \big((RMG + 1) \times 8{,}192 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2\big) \times (RUR + RDR + 2)$$

   (ii) Eliminate the linear deceleration section and reduce the linear acceleration section.

$$RMV \leqq \frac{(RDS + RFL) \times \big(RDS \times (RUR + 2 \times RDR + 3) + RUS \times (RUR + 1)\big) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{and}$$

$$RMV > \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

   Change to S-curve accel/decel (RUS > 0, RDS = 0) without linear deceleration section.

$$RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + 2 \times RDR + 3}$$

However

$$A = RUS \times (RUR + 1)$$
$$B = \left((RMG + 1) \times 8{,}192 \times RMV - 2 \times A \times RFL + (RUR + 2 \times RDR + 3) \times RFL^2\right) \times (RUR + 2 \times RDR + 3)$$

(iii) Eliminate linear accel/decel sections

$$RMV \leqq \frac{(RUS + RFL) \times RUS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

Change to S-curve accel/decel (RUS=0, RDS=0) without linear accel/decel section.

$$RFH \leqq \sqrt{\frac{(RMG + 1) \times 8{,}192 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

3. When RUS > RDS

(i) Reduce linear accel/decel sections.

$$RMV \leqq \frac{(RFH + RFL) \times \left((RFH - RFL) \times (RUR + RDR + 2) + 2 \times RUS \times (RUR + 1) + 2 \times RDS \times (RDR + 1)\right)}{(RMG + 1) \times 8{,}192} \quad \text{and}$$

$$RMV > \frac{(RUS + RFL) \times \left(RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)\right) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

$$RFH \leqq \frac{-A + \sqrt{A^2 + B}}{RUR + RDR + 2}$$

However

$$A = RUS \times (RUR + 1) + RDS \times (RDR + 1)$$
$$B = \left((RMG + 1) \times 8{,}192 \times RMV - 2 \times A \times RFL + (RUR + RDR + 2) \times RFL^2\right) \times (RUR + RDR + 2)$$

(ii) Eliminate linear acceleration section and reduce linear deceleration section

$$RMV \leqq \frac{(RUS + RFL) \times \left(RUS \times (2 \times RUR + RDR + 3) + RDS \times (RDR + 1)\right) \times 4}{(RMG + 1) \times 8{,}192} \quad \text{and}$$

$$RMV > \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

Change to S-curve accel/decel (RUS = 0, RDS > 0) without linear acceleration section.

$$RFH \leqq \frac{-A + \sqrt{A^2 + B}}{2 \times RUR + RDR + 3}$$

However

$$A = RDS \times (RDR + 1)$$
$$B = \left((RMG + 1) \times 8{,}192 \times RMV - 2 \times A \times RFL + (2 \times RUR + RDR + 3) \times RFL^2\right) \times (2 \times RUR + RDR + 3)$$

(iii) Eliminate the linear accel/decel sections.

$$RMV \leqq \frac{(RDS + RFL) \times RDS \times (RUR + RDR + 2) \times 8}{(RMG + 1) \times 8{,}192} \quad \text{at}$$

Change to S-curve accel/decel (RUS = 0, RDS = 0) without linear accel/decel section.

$$RFH \leqq \sqrt{\frac{(RMG + 1) \times 8{,}192 \times RMV}{(RUR + RDR + 2) \times 2} + RFL^2}$$

# 9.4 Examples of speed pattern setting

Example: FL speed = 20 pps, FH1 speed = 110 kpps, Acceleration/deceleration time = 300 ms, Linear acceleration/ deceleration.

1) Reference clock (CLK [Hz]) is 9.8304 MHz.

2) FH1 speed is 110 kpps. Set the speed magnification to 20 times, so that actual speed is 110 kpps or higher.
RMG=59(3Bh)

3) Since the speed magnification is set to 20 times, set RFH1 register value so that FH1 speed becomes 110 kpps.
RFH1=5500(157Ch)

4) Since the speed magnification is set to 20 times, set RFL register value so that FL speed becomes 20 pps.
RFL=1(1h)

5) Since RFH1 register value and RFL register value are set, calculate RUR register value so that accel/decel time becomes 300 ms.

$$UR[s] = \frac{(RFH - RFL) \times (RUR + 1) \times 2}{CLK[Hz]}$$

$$0.3 = \frac{(5500 - 1) \times (RUR + 1) \times 2}{9{,}830{,}400}$$

$$RUR = \frac{9{,}830{,}400 \times 0.3}{(5500 - 1) \times 2} - 1$$

$\therefore$ $\underline{RUR = 267.15 \ \ldots\ldots}$

Only integers can be set in RUR register, so set “267” or “268”.
Actual acceleration/deceleration times are 299.83 ms (RUR=267) or 300.95 ms (RUR = 268).

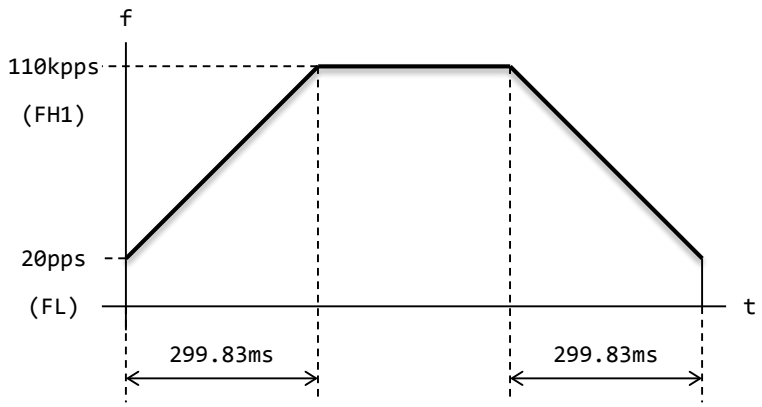



**Fig. 9.4-1 Speed pattern example when “RUR = 267”**

# 9.5 Target speed override

Target speed can be overridden by changing speed register (RFH1, RFH2) during operations.
Serial communication changes byte by byte, which may result in unintended operation due to time differences.

For example, when RFH1 register is changed from “08FFh” to “1000h”, the status of “10FFh” or “0800h” occurs.
Therefore, when overriding the target speed during operation, use RFH1 register and RFH2 register alternately as shown below.

1) Write STAUD1 (43h) command and start from FL speed and accelerate to FH1 speed.
2) Set the new speed data in RFH2 register.
3) Write FSCHH2 (65h) command and override the target speed from FH1 speed to FH2 speed.
4) Set the next new speed data in RFH1 register.
5) Write FSCHH1 (64h) command and override the target speed from FH2 speed to FH1 speed.

When slow-down point is set to “RMD.MSDP = 0” (Auto-setting) due to incremental movement of positioning operations, etc. there are limitations / conditions as follows:

1) Do not change the register value of RFL, RUR, RDR, RUS, RDS, or RMG.
2) Do not override target speeds during S-curve accelerations or deceleration operations.

If these limits are not complied with, a motor can operate at FL speed after deceleration or can stop without decelerating to FL speed.

When performing target speed override during acceleration, set triangle driving to “RMD.MADJ = 1” (Do not avoid).
Speed change commands cannot be used in switch control or pulser control operation modes.

Also, in operation mode of continuous movements by command control, changes in speed pattern differ between linear and S-curve acceleration/deceleration.

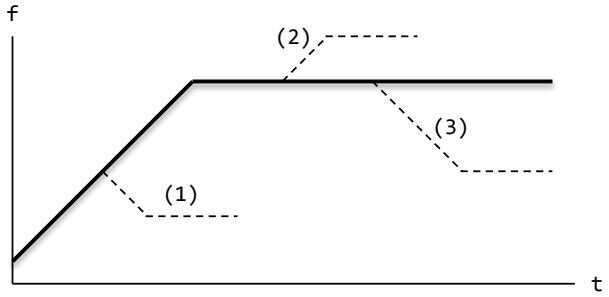



**Fig. 9.5.1 Examples of speed pattern changes due to speed changes during linear accel/decel operations**

| | | |
|---|---|---|
| (1) | Change to RFH2 register during acceleration to FH1 speed: | If changing speed is slower than current speed, the current speed is reduced linearly to the changing speed. |
| (2)(3) | Change to RFH2 register after acceleration to FH1 speed: | Linear acceleration or linear deceleration to the changing speed. |

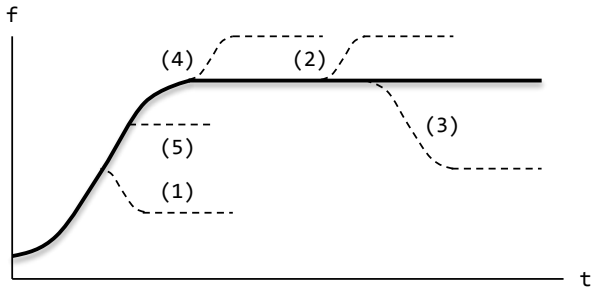



**Fig. 9.5.2 Examples of speed pattern changes due to speed changes during S-curve accel/decel operation**

| | | |
|---|---|---|
| (1) | Change to RFH2 register during acceleration to FH1 speed: | If “FH2 speed < current speed”, S-curve deceleration to FH2 speed. |
| (5) | Change to RFH2 register during acceleration to FH1 speed: | If “FH2 speed≧current speed”, the speed is accelerated to FH2 speed without changing the S-curve characteristic. |
| (4) | Change to RFH2 register during acceleration to FH1 speed: | If FH2 speed > FH1 Speed, accelerate to FH1 speed without changing the S-curve characteristics, and then re-accelerate to FH2 speed. |
| (2)(3) | Change to RFH2 register after acceleration to FH1 speed: | S-curve accelerates or S-curve decelerates to FH2 speed. |

# 10. Function description

## 10.1 Output pulse control

### 10.1.1 Output pulse mode and direction change timer

There are total eight types of command pulse output modes for selection; four types of “common pulse mode”, two types of “2-pulse mode” and two types of “90-degree phase difference mode”.

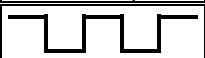
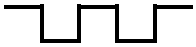
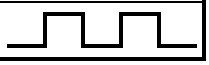
Common pulse mode: Outputs the operation pulse from OUT terminal.
Direction (determination) signal is output from DIR terminal.
(RENV.PMD = 000b to 011b)

2-pulse mode: Outputs pulses for positive direction operation from OUT terminal.
Outputs pulses for negative direction operation from DIR terminal.
(RENV.PMD = 100b, 111b)

90-degree phase difference mode: Outputs A-phase pulse signals with 90-degree phase difference from OUT terminal by 4x.
Outputs B-phase pulse signals with 90-degree phase difference from DIR terminal by 4x.
One 90-degree phase difference pulse corresponds to one pulse in common or 2-pulse mode.
(RENV.PMD = 101b, 110b)

Output mode of command pulse is set by RENV1.PMD bit.

If a motor driver with common pulse mode requires the time from change of direction determination signal to a receipt of command pulse, “direction change timer” can be used.
If “RENV1.DTMF = 0” is set, operation starts can be postponed for 0.2 ms (direction change timer) from the change of direction determination signals. If not required, set “RENV1.DTMF = 1”.

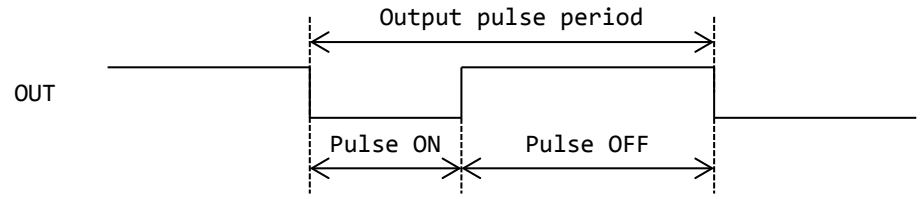
| Output pulse specification | | | | | RENV1.PMD(2 to 0) |
|---|---|---|---|---|---|
| PMD | Positive (+) direction operation | | Negative (−) direction operation | | |
| | OUT output | DIR output | OUT output | DIR output | |
| 000 |  | High |  | Low | |
| 001 |  | High |  | Low | |
| 010 |  | Low |  | High | |
| 011 |  | Low |  | High | |
| 100 |  | High | High |  | |
| 101 | OUT  DIR  | | OUT  DIR  | | |
| 110 | OUT  DIR  | | OUT  DIR  | | |
| 111 |  | Low | Low |  | |
| 101 and 110 correspond to 4x only. | | | | | |
| Direction change timer function<br>0: Enable. Delays the start of operation for 0.2 ms.<br>1: Disable. | | | | | RENV1.DTMF(15) |

## 10.1.2 Output pulse width and operation complete timing

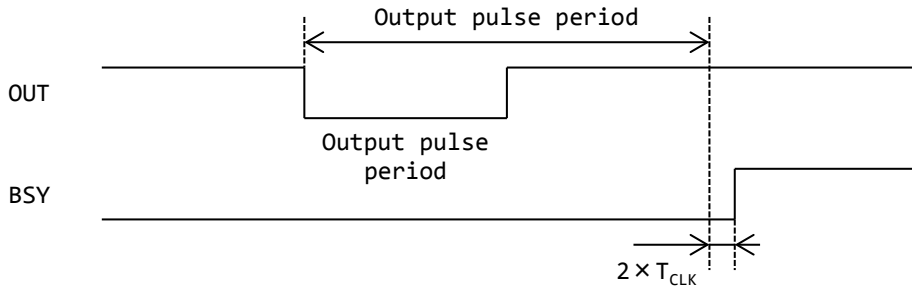
The duty ratio of output pulse ON time width is 50%.
When RMG register value is an even number, a duty error occurs. ON time becomes shorter than OFF time as shown in the following equation.

$$\frac{Pulse\ ON\ time}{Output\ pulse\ cycle} = \frac{\frac{RMG}{2}}{RMG+1}$$

For example, when RMG = 4, the output pulse cycle is 5 and the pulse ON time is 2. So the duty ratio becomes 2:3.




This chart indicates the timing of BSY changes when the operation is completed.



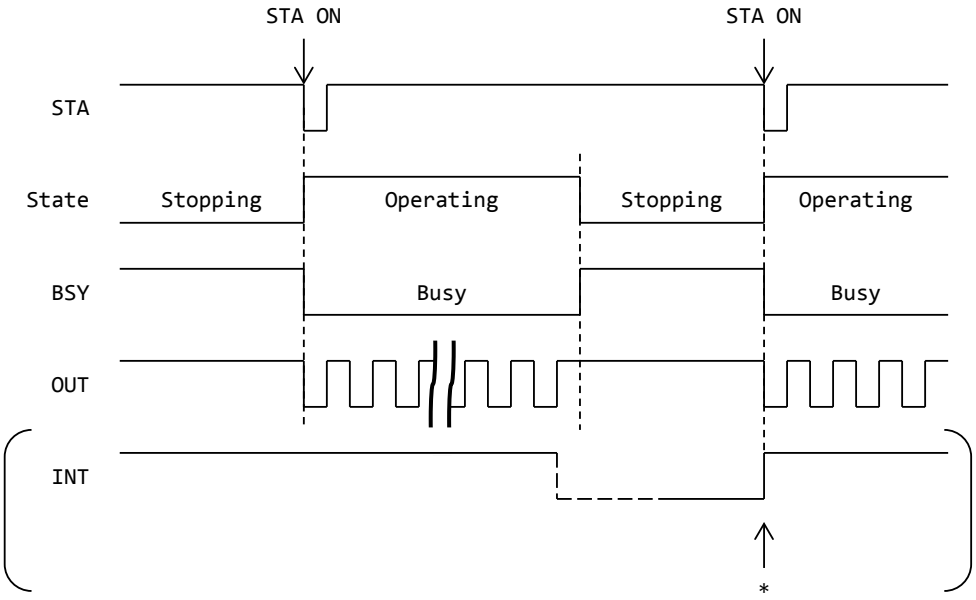

($T_{CLK}$: reference clock cycle)

# 10.2 Operation state check output

BSY or END signal can be output by setting RENV1.ENDM bits.
For servo motor control, “RMD.MINP = 1” (INP signal input is enabled) can be set to delay the completion of operation until INP signal is input.

## 10.2.1 BSY signal

When “RENV1.ENDM = 0”, BSY signal indicates that the operation mode is in operation.

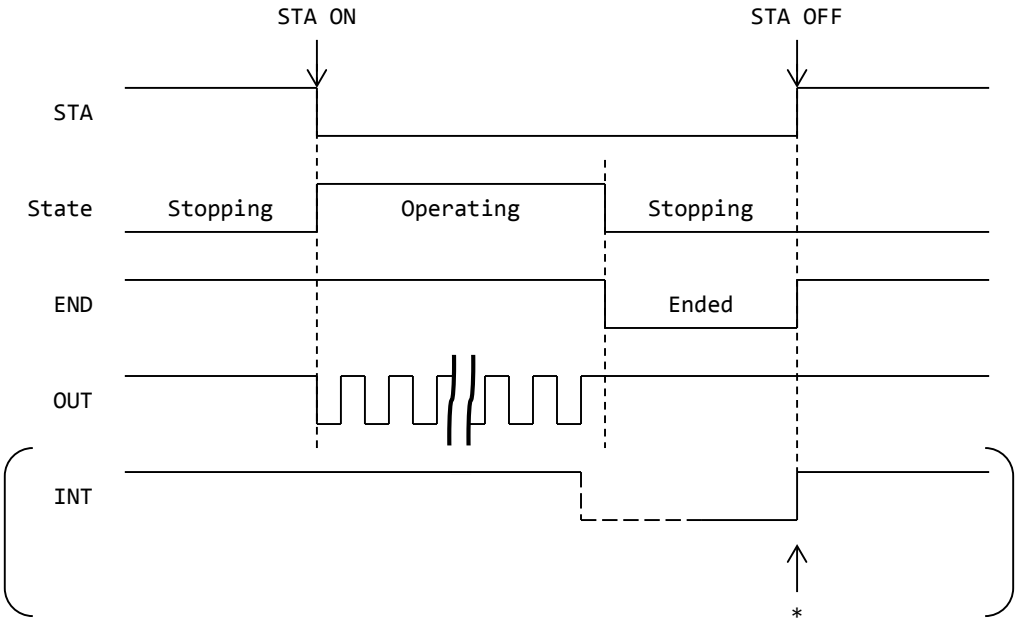



* In the case of stand-alone operation, even if INT signal is output for some reason, it is automatically cleared at this timing.

## 10.2.2 END signal

When “RENV1.ENDM = 1” is set, a signal indicating the completion of operation is output.

In stand-alone operation without using CPU, an operation can be started with STA signal input.
When the operating time is short, BSY signal width is also shortened, so that it may not confirm the movement.
In this case, END signal and STA signal can be used for handshake control.




* In the case of stand-alone operation, even if INT signal is output for some reason, it is automatically cleared at this timing.

To perform handshake control, confirm the following operations.

1. Set “RENV1.STAM = 1” (edge-triggered) and “RENV1.ENDM = 1” (END signal).
2. Add “RMD.MSY=1” (waiting for STA-signal input) to operation mode and write Start command.
3. Change STA signal from “H level” to “L level” and start.
4. When operation mode is completed, END signal becomes “L level”.
5. Change STA signal from “L level” to “H level” to end.

Operation can be confirmed by operating STA signal like this.

| | |
|---|---|
| MODE<br>0: CPU-connected system.<br>1: Stand-alone operating mode. | MODE terminal |
| INP signal input<br>0: Disable.<br>1: Enable. | RMD.MINP(9) |
| INP signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.INPL(11) |
| Output selection of BSY/END terminal<br>0: BSY signal.<br>1: END signal. | RENV1.ENDM(14) |

# 10.3 Idling control

When starting acceleration/deceleration operations with stepping motors, acceleration can be started after several pulses are output at FL speed. This reduces occurrence of out-of-step due to rapid acceleration. These are called “idling pulses”.
The number of idling pulse is set to RENV1.IDL bit.

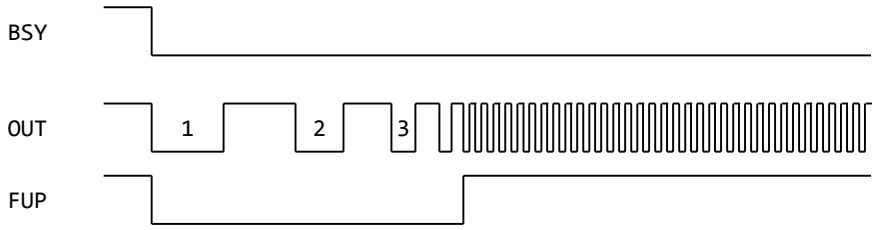
When this function is not used, set the setting value “n” to “0” or “1”.
Acceleration starts at the same time as command pulse output. The initial speed that is calculated by the cycle of the first two pulses is faster than FL-speed.

When using this function, set the value “n” from “2” to “7”.
Acceleration starts at the timing when the nth pulse is output.
Initial speed becomes FL speed, and the FL speed can be set close to the upper limit of starting pulse rate of a stepping motor.
The number of idling pulse to be output at FL speed becomes “n − 1” pulse.

Even if this function is used in an operation mode of incremental movement, the total number of output pulses does not change.

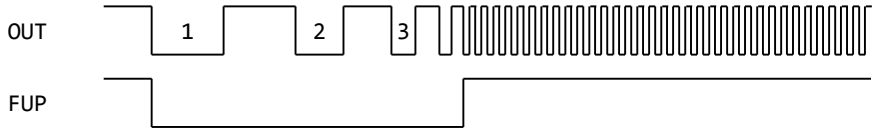
[Relationship between Setting of Idling Pulse Number and Acceleration Start Timing]

RENV1.IDL = 0



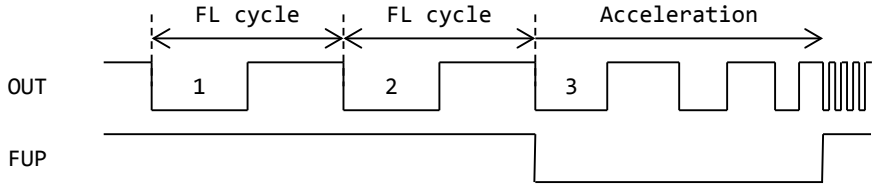

▲ Start of acceleration from the 0th pulse.
(Idling pulse output: disabled )

RENV1.IDL = 1




▲ Start of acceleration from the 0th pulse.
(idling pulse output: RENV1.IDL – 1 = 0)

RENV1.IDL = 3




Start of acceleration from the third pulse. ▲
(Idling pulse output: RENV1.IDL – 1 = 2)

| | |
|---|---|
| Idling pulse count<br>0: Idling pulse output disabled.<br>n: Idling pulse output enabled. n = 1 to 7.<br>“n - 1” is the number of output idling pulse. | RENV1.IDL(30~28) |

# 10.4 External mechanical signal input

## 10.4.1 PEL and MEL signals

When EL signal is turned on during operation, immediate stop or deceleration stop is performed.
Even if EL signal is turned OFF after stopping, the movement remains stopped.
When EL signal of the moving direction turns OFF, the movement can be started in the same moving direction.
For your safety, it is recommended that EL signal should maintain ON up to the end of stroke.

Immediate stop or deceleration stop (FH high-speed start only) can be selected when EL signal input is ON by setting RENV1.ELM bit.
However, when decelerates and stops, the movement stops after passing the end limit position. The passing amount changes depending on the speed setting. Make sure that there are no mechanical problems for this.

The smallest pulse width of EL signal is 4 µs when the filter is ON.
Turn OFF the input filter to set to 0.1 µs width.

EL terminal can be monitored by reading RSTS.SMEL and RSTS.SPEL bits.
By reading RIST.IMEL bit and RSTS.IPEL bit, it is possible to monitor the interrupt factor caused by turning ON EL terminal.

During timer operation mode, EL signal is ignored.
During the mode, EL signal can be monitored by reading RSTS register.

The input logic of PEL signal can be set using PELL terminal.
The input logic of MEL signal can be set using MELL terminal.

In pulser control operation, a difference of 1 pulse or more may be generated between number of manual pulser signals and number of output pulse signals when escaping from end limit position in reverse operation.

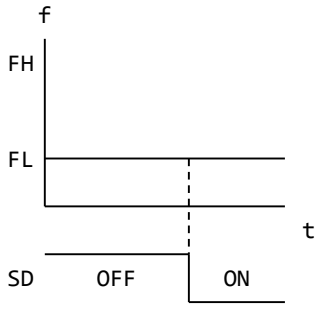
| | |
|---|---|
| PEL signal logic<br>L: Positive logic.<br>H: Negative logic. | PELL external terminal |
| MEL signal logic<br>L: Positive logic.<br>H: Negative logic. | MELL external terminal |
| EL signal of operation directions<br>0: Immediate stop.<br>1: Decelerate and stop. (Immediate stop when the speed pattern is “constant-speed”). | RENV1.ELM(3) |
| PEL terminal status<br>0: OFF.<br>1: ON. | RSTS.SPEL(18) |
| MEL terminal status<br>0: OFF.<br>1: ON. | RSTS.SMEL(17) |
| EL signal input filter<br>0: Recognizes signals with a pulse width of 0.1 µs or wider.<br>1: Recognizes signals with a pulse width of 4 µs or wider. | RENV1.FLTR(12) |

## 10.4.2 SD signal

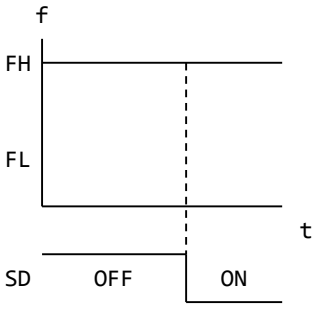
When “RMD.MSDE = 0”, SD signals are ignored.
When “RMD.MSDE = 1”, the movement will (1) decelerate, (2) latch & decelerate, (3) decelerate and stop, and (4) latch & decelerate and stop if SD signal turns ON.

1) Deceleration <RENV1.SDM = 0, RENV1.SDLT = 0>
- For constant-speed patterns, SD signals are ignored.
- For high-speed patterns, movement will slow down to FL speed when SD signal turns ON.
  It will accelerate to FH speed if SD signal turns OFF after deceleration or during deceleration.
- If STAUD1 (43h) command or STAUD2 (44h) command is written, and if SD signal is ON, the movement operates at FL speed.
  When SD signal turns OFF, the movement will accelerate to FH speed.

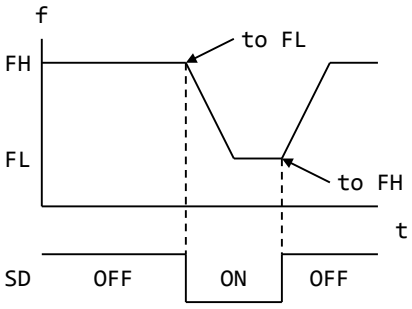
[FL constant-speed pattern]




[FH constant-speed pattern]

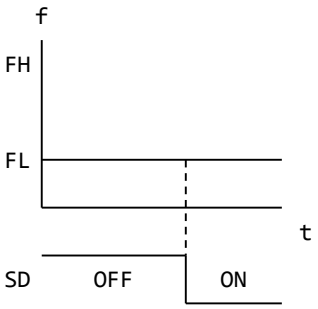



[FH high-speed pattern]

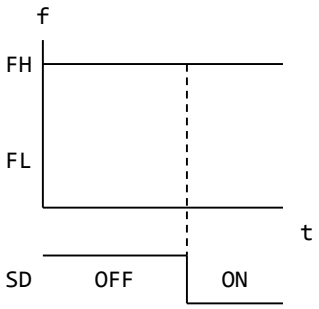



2) Latch & deceleration <RENV1.SDM = 0, RENV1.SDLT = 1>
- For constant-speed patterns, SD signals are ignored.
- For high-speed patterns, the movement will slow down to FL speed when SD signal turns ON.
- Even if SD signal turns OFF after deceleration or during deceleration, FL speed is maintained and the movement will not accelerated to FH speed.
- When STAUD1 (43h) command or STAUD2 (44h) command is written and while SD signal is ON, the movement will operate at FL
- speed.
  Even if SD signal turns OFF, the movement will not accelerate to FH speed.
- SD latched signal becomes SD signal input status at the time of the next start command writing.

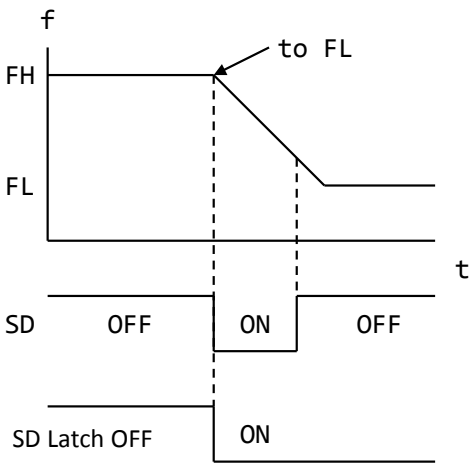
[FL constant-speed patterns]




[FH constant-speed patterns]

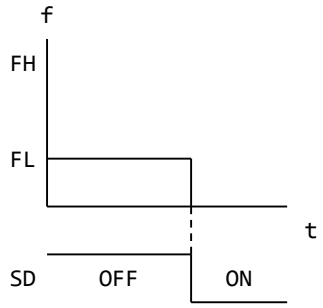



[FH high-speed pattern]

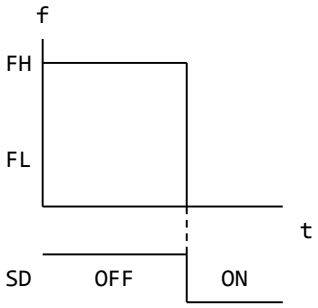


3) Deceleration stop <RENV1.SDM = 1, SDLT = 0>
- For constant-speed patterns, the movement will stop immediately when SD signal turns ON.
- For high-speed patterns, the movement will decelerate to FL speed and stop when SD signal turns ON.
  When SD signal turns OFF while decelerating, the movement will accelerate to FH speed.
- It remains stopped even if SD signal turns OFF after deceleration stop.
- If SD signal is ON at writing a start command, the operation is completed without starting.
- An interrupt is generated when stopped.

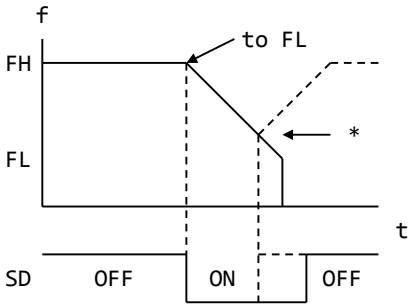
[FL constant-speed pattern]




[FH constant-speed pattern]



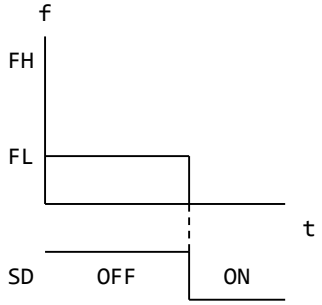

[FH high-speed pattern]



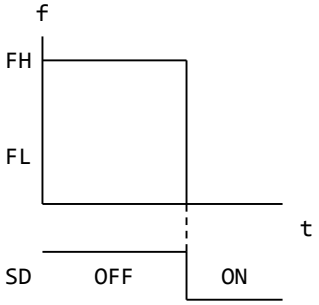

* Re-accelerate to FH when SD signal turns OFF during deceleration

4) Latch & deceleration stop <RENV1.SDM = 1, SDLT = 1>
- For constant-speed patterns, the movement will stop immediately when SD signal turns ON.
- For high-speed patterns, it will decelerate to FL speed and will stop when SD signal turns ON.
  It will not accelerate even if SD signal turns OFF during deceleration.
- If SD signal is ON at writing a start command, the operation is completed without starting.
- An interrupt is generated when stopped.

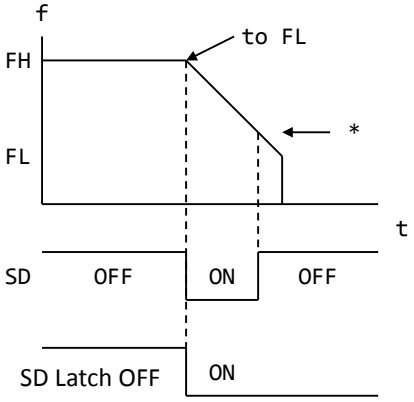
[FL constant-speed pattern]




[FH constant-speed pattern]




[FH high-speed pattern]




* SD signals OFF is disabled during deceleration.

SD latch signal is reset even if SD latch signal is set to “RENV1.SDLT = 0”.
The minimum pulse width of SD signal is 4 µs when the input-filter is ON, but the width becomes 0.1 µs when the input-filter is OFF.
SD signal status can be monitored by RSTS.SDIN bit.
The latch status of SD signal can be monitored by RSTS.SSD bit.
Interrupt factor at the stop by SD signal turning ON can be monitored by RIST.ISSD bit.

| | |
|---|---|
| SD signal input<br>0: Disabled.<br>1: Enabled. | RMD.MSDE(6) |
| SD signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.SDL(6) |
| When SD signal turns ON<br>0: Decelerate.<br>1: Decelerate and stop. Immediate stop when the speed pattern is “constant-speed”. | RENV1.SDM(4) |
| SD signal latching<br>0: Disabled.<br>1: Enabled.<br>If SD signal input is turned OFF, latch status turns OFF when an operation starts.<br>Writing “RENV1.SDLT = 0”, latch status turns OFF. | RENV1.SDLT(5) |
| SD signal latched state<br>0: OFF.<br>1: ON. | RSTS.SSD(19) |
| SD terminal state<br>0: OFF.<br>1: ON. | RSTS.SDIN(20) |
| Reading the interrupt factor when stopped by SD signal<br>1: Stopped by SD signal ON. | RIST.ISSD(3) |
| Input-filter of SD signal<br>0: Recognize signals with a pulse width of 0.1 μs or wider.<br>1: Recognize signals with a pulse width of 4 μs or wider. | RENV1.FLTR(12) |

## 10.4.3 ORG signal and EZ signal

ORG signal and EZ signal are enabled in the operation mode of origin signal control (Origin return, limited origin return and origin escape).
Operation mode and moving direction are set in RMD register.
ORG signal is sampled at rising edge of output pulse when the logic of output pulse is negative.
The smallest pulse width of ORG signal requires additional one cycle of output pulse to the input filter time.
ORG signal inputs are latched internally and reset when stopped.

The logic of ORG signal can be changed by RENV1.ORGL bit.
The state of ORG terminal can be monitored by RSTS.SORG bit.

The logic of EZ signal can be changed by RENV2.EZL bit.
The state of EZ terminal can be monitored by RSTS.SEZ bit.

For details on origin signal control, see “8.2 Origin signal control: Origin return”.

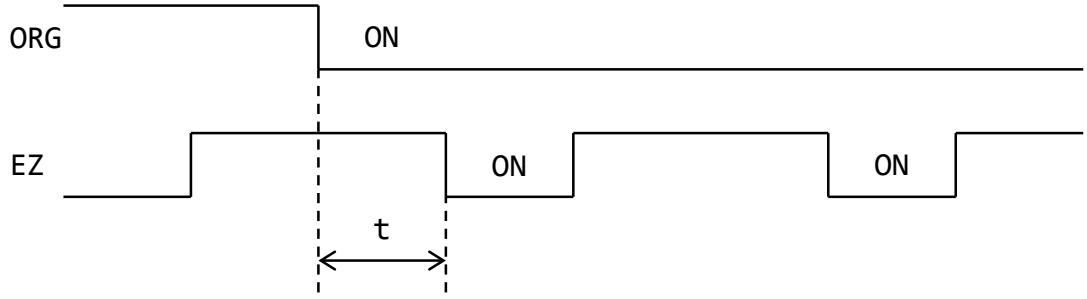



**Fig. 10.4-1 Timing of ORG signal and EZ signal**

(i) When $t \geqq 4 \times T_{CLK}$ ... Count
(ii) When $T_{CLK} < t < 4 \times T_{CLK}$ ... Whether or not to count is uncertain
(iii) When $t \leqq T_{CLK}$ ... Do not count

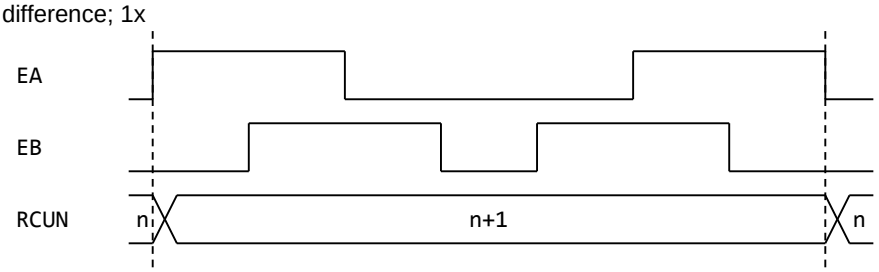
($T_{CLK}$: reference clock cycle)

| | |
|---|---|
| Operation mode to enable ORG signal and EZ signal<br>0001: Origin return operation.<br>0010: Origin return operation with feeding amount limit.<br>0011: Origin escape operation. | RMD.MOD(3 to 0) |
| ORG signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.ORGL(7) |
| ORG terminal state<br>0: OFF.<br>1: ON. | RSTS.SORG(21) |
| Input filter of ORG signal<br>0: Recognizes signals with a pulse width of 0.1 µs or wider.<br>1: Recognizes signals with a pulse width of 4 µs or wider. | RENV1.FLTR(12) |
| Number of EZ signal count<br>Sets the origin return operation completion condition and the number of EZ counts in operation for EZ counts.<br>Set (count − 1) value to RENV2.EZD bit.<br>The set value ranges from “0” to “15”. | RENV2.EZD(7 to 4) |
| EZ signal logic<br>0: Negative logic (count at falling edge).<br>1: Positive logic (count at rising edge). | RENV2.EZL(3) |
| EZ terminal state<br>0: OFF.<br>1: ON. | RSTS.SEZ(7) |
| Input-filter of EZ signal<br>0: Recognizes signals with a pulse width of 0.1 µs or wider.<br>1: Recognizes signals with a pulse width of 0.3 µs or wider. | RENV2.EINF(10) |

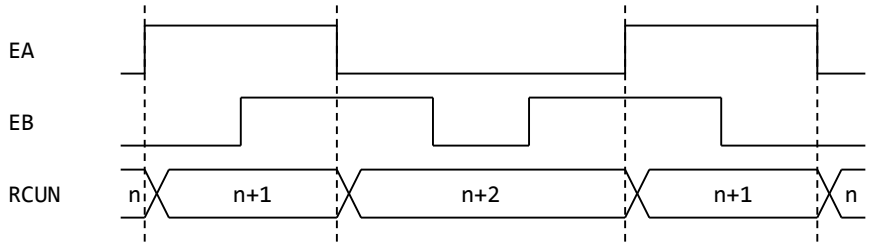
## 10.4.4 EA and EB signals

EA and EB signals are used as signals to indicate the mechanical position by encoders.
The input methods of EA signal and EB signal are specified by RENV2.EIM bit.
The input count timings of EA signal and EB signals are shown below.

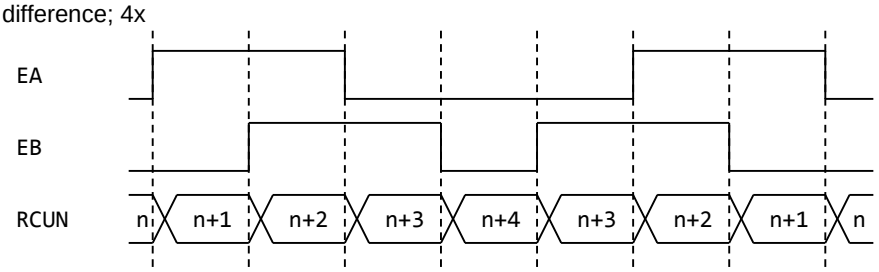
1) 90-degree phase difference; 1x



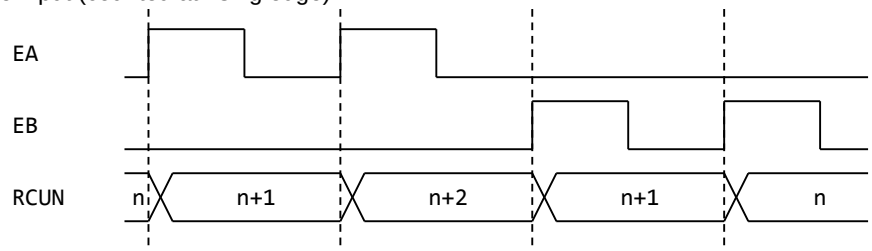

2) 90-degree phase difference; 2x




3) 90-degree phase difference; 4x




4) Up/down of 2-pulse input (counted at rising edge)




With RENV2.EIM bit, the input methods of EA and EB signals are as follows:

| EIM | Operation |
|---|---|
| 00 | Input with 90-degree phase difference; 1x. |
| 01 | Input with 90-degree phase difference; 2x. |
| 10 | Input with 90-degree phase difference; 4x. |
| 11 | Count up at rising edge of EA signal; count down at rising edge of the EB signal. |

# 10.5 Servo motor I/F

## 10.5.1 INP signal

Pulse train input type servo drivers have the internal deviation counters.
The deviation counter counts differences between command pulse inputs and feedback pulse input.
A servo driver controls a motor so that the difference between command pulse inputs and feedback pulse input becomes “0”.
Therefore, a servo motor operates behind the command pulse.
As a result, even if the command pulse stops, motor stopping will be delayed until the deviation counter in the driver reaches “0”.

PCD2112A can change the timing of completion of operation to the timing when the positioning completion signal (INP signal) from the servo driver is input. At this time, the change of BSY signal due to the completion of operation occurs when INP signal is input.

If INP signal is ON before pulse output is completed, the operation will be completed without delay.

The logic of INP signal can be changed with RENV1.INPL bit.
INP terminal can be monitored by RSTS.SINP bit.

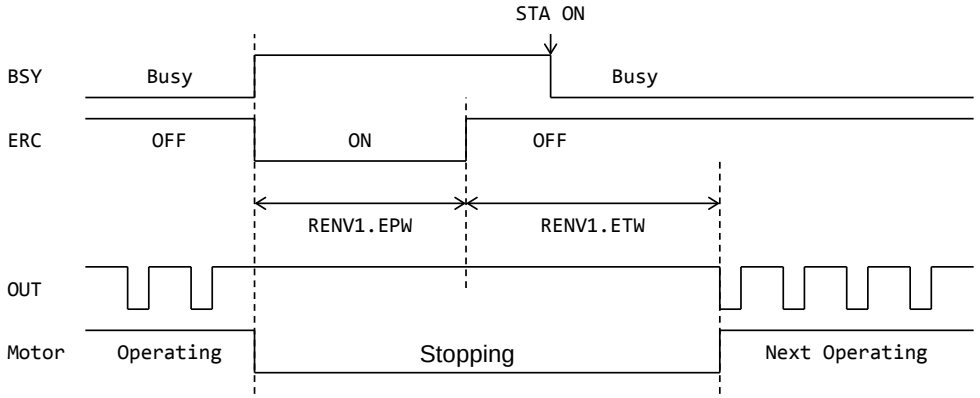
The minimum pulse width of INP signal is 4 μs when the input filter is ON.
It becomes 0.1 μs when the input-filter is OFF.

| | |
|---|---|
| Operation completion delay due to INP signal<br>0: No operation completion delay due to INP signal.<br>1: Operation completion is delayed until INP signal turns ON. | RMD.MINP(9) |
| INP signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.INPL(11) |
| INP terminal state<br>0: OFF.<br>1: ON. | RSTS.SINP(22) |
| Input filter for INP signal<br>0: Recognizes signals with a pulse width of 0.1 μs or wider.<br>1: Recognizes signals with a pulse width of 4 μs or wider. | RENV1.FLTR(12) |

## 10.5.2 ERC signal

Even if command pulse is stopped, operation stop will be delayed until deviation counter in the driver reaches “0”.
The deviation counter must be cleared to zero to stop a servo motor immediately such as origin return.
If “RENV1.CDWS = 0” is set, ERC signal can be output to clear the deviation counter to zero in a servo motor driver.

Select one-shot signal or level signal for ERC signal.
Use RENV1.EPW bit to select the output width.
The time from when ERC signal goes to H level (=OFF) until the servo driver receives command pulse is OFF-timer time.
OFF timer time is selected with RENV1.ETW bit.




Set “RENV1.EROR = 1” to output ERC signal when origin return movement is completed.
Set “RENV1.EROE = 1” to output ERC signal when stopped immediately by EL signal or emergency stop command.
ERC signal can also be output by writing ERC signal output command (ERC0).
ERC signal logic can be changed by RENV1.ERCL bits.
ERC terminal state can be monitored by RSTS.SERC bits.

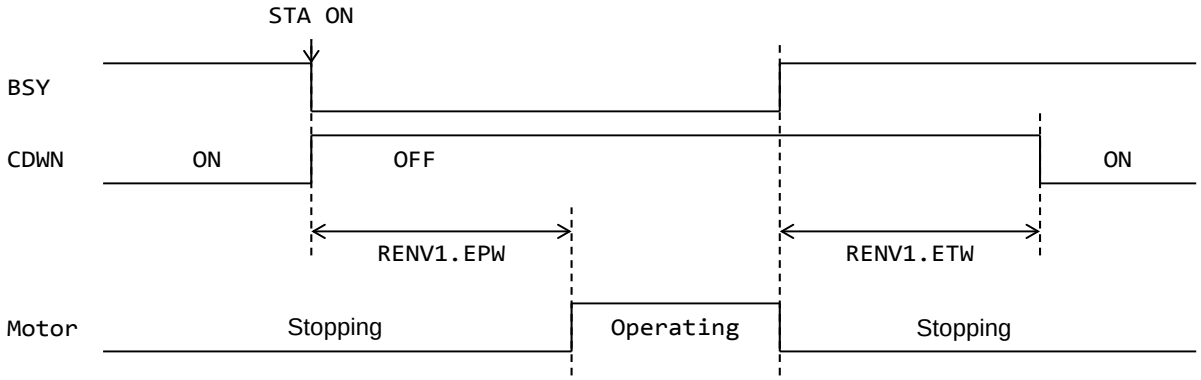
| | |
|---|---|
| ERC/CDW terminal output<br>0: ERC signal.<br>1: CDW signal. | RENV1.CDWS(23) |
| ERC signal output due to abnormal stop<br>0: Disabled.<br>1: Enabled.<br>ERC signal is output when an operation immediately stops with EL signal or emergency stop command.<br>ERC signal is not output at deceleration stop. | RENV1.EROE(24) |
| ERC signal output due to origin return<br>0: Disabled.<br>1: Enabled.<br>Automatically outputs ERC signal when the origin return operation is completed.<br>ERC signal is also output at deceleration stop. | RENV1.EROR(25) |
| Output width of ERC signal<br>000: 12 µs 001: 102 µs 010: 409 µs 011: 1.6 ms<br>100: 13 ms 101: 52 ms 110: 104 ms 111: Level output | RENV1.EPW(18 to 16) |
| Output logic of ERC signal<br>0: Negative logic.<br>1: Positive logic. | RENV1.ERCL(19) |
| ERC signal OFF timer time<br>000: 0 µs 001: 12 µs 100: 1.6 ms 110: 52 ms<br>101: 104 ms 011: 208 ms 101: 416 ms 111: 832 ms | RENV1.ETW(22 to 20) |
| ERC terminal state<br>0: OFF.<br>1: ON. | RSTS.SERC(23) |
| ERC signal output command<br>Outputs ERC signal. | ERCO(10h) |
| ERC signal reset command<br>Turns OFF ERC signal when the output width is level output. | ERCR(11h) |

# 10.6 Stepping motor I/F

## 10.6.1 CDW signal

When “RENV1.CDWS = 1” is set, current down signal (CDW signal) can be output from ERC/CDW terminal.

RENV1.EPW bit is delay time from the end of current down to the start of operation.
RENV1.ETW bit is delay time from the end of operation to the start of current down.




| | |
|---|---|
| Output of ERC/CDW terminal<br>0: ERC signal.<br>1: CDW signal. | RENV1.CDWS(23) |
| Time from the end of current down to start of operation (current up timer)<br>000: 12 µs 001: 102 µs 010: 409 µs 011: 1.6 ms<br>100: 13 ms 101: 52 ms 110: 104 ms 111: OFF * | RENV1.EPW(18 to16) |
| Time from the end of operation to start of the current down (current down timer)<br>000: 0 µs 001: 12 µs 010: 1.6 ms 011: 52 ms<br>101: 104 ms 100: 208 ms 110: 416 ms 111: 832 ms | RENV1.ETW(22 to 20) |
| CDW signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.ERCL(19) |

* Even if “RENV1.CDWS = 1” is set, CDW signal is fixed to OFF when “RENV1.EPW = 111b”

Note: When the next operation starts within the time of current down timer (RENV1.ETW bit), CDW signal does not turn ON and operation starts after the time of current up timer (RENV1.EPW bit).

## 10.6.2 PH1 to PH4 signals

The excitation sequences of 2-phase stepping motors can be output.
The excitation method can be selected from full step (L) and half step (H) by setting FH terminal
The driving method can be selected from unipolar drive (L) and bipolar drive (H) by setting UB terminal.

[Unipolar drive]

| Full-step (2-2 phase excitation) | | | | | |
|---|---|---|---|---|---|
| step→ | 0 | 1 | 2 | 3 | 0 |
| PH1 | H | H | L | L | H |
| PH2 | L | H | H | L | L |
| PH3 | L | L | H | H | L |
| PH4 | H | L | L | H | H |
| Negative ← Moving direction → Positive | | | | | |

| Half-step (1-2 phase excitation) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| step→ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| PH1 | H | H | H | L | L | L | L | L | H |
| PH2 | L | L | H | H | H | L | L | L | L |
| PH3 | L | L | L | L | H | H | H | L | L |
| PH4 | H | L | L | L | L | L | H | H | H |
| Negative ← Moving direction → Positive | | | | | | | | | |

Note 1: When “RENV1.PHMA = 1” is set, the excitation sequence output becomes “PH1 to PH4 = LLLL” while CDW signal is being output.
When “RENV1.PHMK = 1” is set, the excitation sequence outputs become “PH1 to PH4 = LLLL”.

[Bipolar drive]

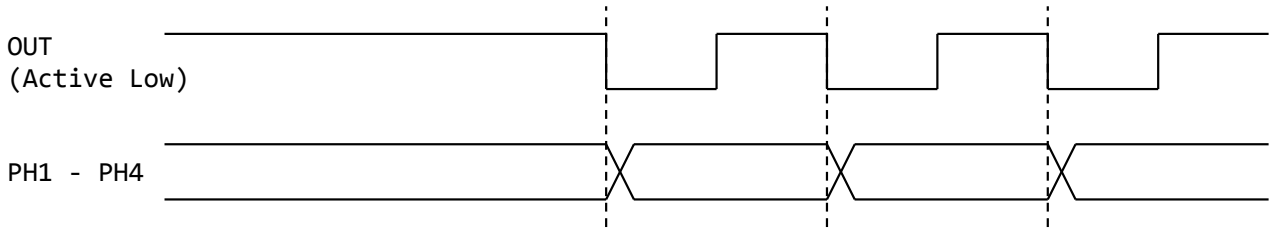
| Full-step (2-2 phase excitation) | | | | | |
|---|---|---|---|---|---|
| Step→ | 0 | 1 | 2 | 3 | 0 |
| PH1 | H | H | L | L | H |
| PH2 | L | H | H | L | L |
| PH3 | L | L | L | L | L |
| PH4 | L | L | L | L | L |
| Negative ← Moving direction → Positive | | | | | |

| Half-step (1-2 phase excitation) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Step→ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| PH1 | H | H | H | H | L | L | L | L | H |
| PH2 | L | L | H | H | H | H | L | L | L |
| PH3 | L | L | L | H | L | L | L | H | L |
| PH4 | L | H | L | L | L | H | L | L | L |
| Negative ← Moving direction → Positive | | | | | | | | | |

Note 2: When “RENV1.PHMA = 1” is set, the excitation sequence output becomes “PH1 to PH4 = LLHH” while CDW signal is being output.
When “RENV1.PHMK = 1” is set as well, the excitation sequence outputs becomes “PH1 to PH4 = LLHH”.

PH1 to PH4 terminal states can be monitored with RSTS.SPH1 to SPH4 bit.

The sequence is switched per the following timing:



# 10.7 External start and simultaneous start

## 10.7.1 STA signal in CPU-connected system

PCD2112A can start by an external STA signal using STA terminal.
When “RMD.MSY = 1” is set, the operation starts at the timing of “STA = L level”.

Multiple PCD2112A can be used for multiple axis control.
Connects the STA terminal of each LSI, write a start command to each LSI, and then input the same STA signals.
This will start multiple axes with the state of “RSTS.SCM = 0010” (waiting for STA signal input) simultaneously.
STA signal can be output from STA terminal by STAO (12h) command instead of external STA signal.

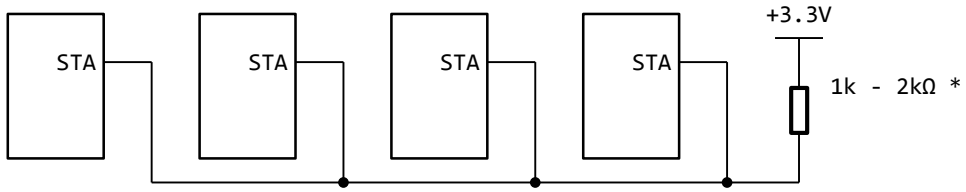
If “RENV2.ESTA = 1” is set, interrupt can be generated when a simultaneous start (STA signal input is ON) is performed.
The interrupt factor can be checked with RIST.ISTA bits.

The logic of STA terminal cannot be changed.
The state of STA terminal can be monitored by RSTS.SSTA bits.

Level trigger input and Edge trigger input can be selected as the input method of STA signal.
When level trigger input is selected with “STA = L level”, writing a start command starts an operation immediately.

Even if STA terminals of several PCD2112A are connected each other, each axis can be started independently by start command. To cancel “RSTS.SCM=0010” (waiting for STA signal input), write STOP (31h) command.

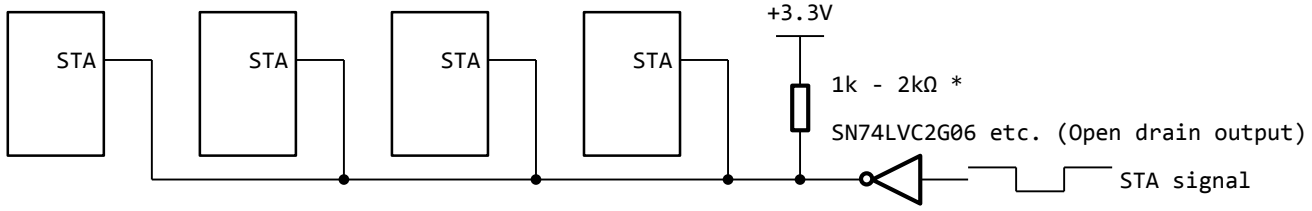
< Simultaneous start >
1) To perform a simultaneous start of multiple PCD2112As, connect as follows.




* STA terminal contains a pull-down resistor with a minimum of 40 kΩ.

2) After setting “RMD.MSY = 1” to the axis to start, write a start command to make it “RSTS.SCM = 0010” (waiting for STA signal input).
3) 0.8 µs wide one-shot signal is output from STA terminal by STAO (12h) command.
When using STAO (12h) command, select “RENV2.STAF = 0”.

< External start >
1) To perform a simultaneous start from an external circuit, connect as follows.




* STA terminal contains a pull-down resistor with a minimum of 40 kΩ.

2) After setting “RMD.MSY = 1” to the axes to start, write a start command so that the axes become “RSTS.SCM = 0010” (waiting for STA signal input) state.
3) Input one-shot signals from outside.
Drive external STA signals with open drain outputs (SN74LVC2G06, etc.) before inputting.

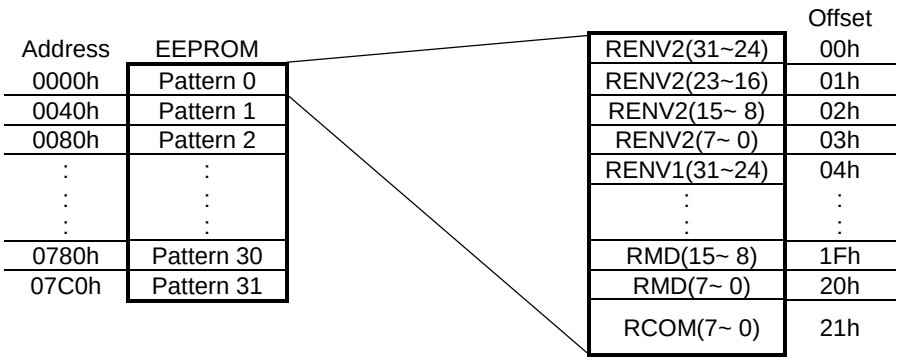
Input one-shot signal of 0.5 µs or wider to STA signal when “RENV2.STAF = 0” is set.
Input one-shot signal of 40 ms or wider to STA signal when “RENV2.STAF = 1” is set.

When “RENV1.ENDM = 1” (END signal) is used, select “RENV1.STAM = 1” (edge-triggered) for STA signal.
Be sure to maintain “STA = L level” state until END becomes “L level”.

| | |
|---|---|
| Waiting for STA signal input<br>0: Start immediately.<br>1: Start by STA signal input. | RMD.MSY(12) |
| STA signal type<br>0: Level trigger.<br>1: Edge trigger. | RENV1.STAM(13) |
| Input noise filter at STA terminal<br>0: Recognize signals with a pulse width of 0.5 µs or wider.<br>1: Recognize signals with a pulse width of 40 ms or wider. | RENV2.STAF(15) |
| STA terminal state<br>0: OFF.<br>1: ON. | RSTS.SSTA(29) |
| Operation state<br>0010: Waiting for STA signal input. | RSTS.SCM(27 to 24) |
| Interrupt operation by STA signal<br>0: Disabled.<br>1: Enabled.<br>Note: It cannot be used in a stand-alone operation. | RENV2.ESTA(19) |
| Interrupt operation by STA signal<br>0: Not occurred.<br>1: Occurred.<br><br>When “RENV1.STAM = 1” and “STA = L level”, operation mode does not start even if a start command is written. However, the interrupt condition is satisfied, “RIST.ISTA = 1” is obtained. | RIST.ISTA(9) |
| Output command of STA signal<br>Outputs a one-shot signal of 0.8 µs from STA terminal. | STAO(12h) |

## 10.7.2 STA and PS0-PS4 signals in stand-alone operations

In a stand-alone operation, PCD2112A operates by storing operation modes in an external four-wire serial EEPROM.
In an operation, the EEPROM needs to be 2k byte or more.
The EEPROM can store operation patterns (setting values to the registers) for multiple PCD2112As as follows.

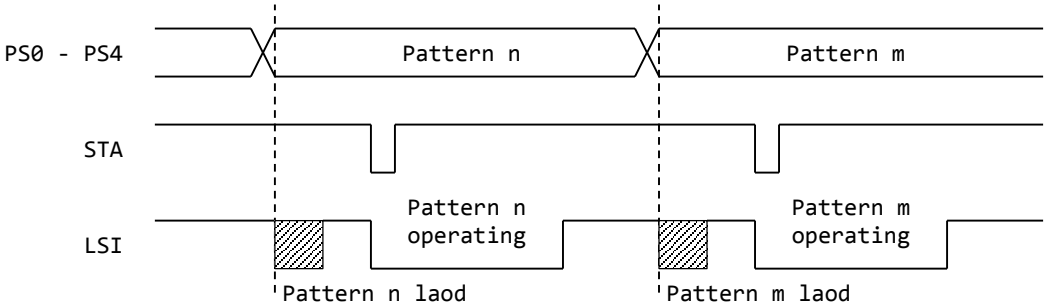



Note: Register deployment of operation pattern is the same as "4.1 Detailed memory map".
Set the operation patterns from RENV1 register to the RCOM register as one unit.

The operation pattern to be used is determined by external terminals PS0 to PS4.

| PS4 - PS0 | Select Pattern |
|---|---|
| 00000 | Pattern 0 |
| 00001 | Pattern 1 |
| : | : |
| 11110 | Pattern 30 |
| 11111 | Pattern 31 |

When the terminal states from PS0 to PS4 change, PCD2112A reads the operation pattern selected by EEPROM.
At this time, the start command of RCOM register is also read, and operates immediately.
When “RMD.MSY = 1” is set for the operation pattern, input of STA signal is awaited.
For continuous movements by switch control or pulser control, “RMD.MSY = 0” is also OK because input signals to PA/PDR or PB/MDR terminals are awaited.




When “RENV1.ENDM = 1” (END signal) is used, select “RENV1.STAM = 1” (edge-triggered) for STA signal.
Be sure to maintain “STA = L level” until END becomes “L level”.

Immediate stop is conducted when the states of PS0 to PS4 terminals changes during operation.
After that, LSI starts reading a new operation pattern.

# 10.8 External stop

## 10.8.1 STP signal

PCD2112A can perform immediate stops or deceleration stops using external STP signal inputs through STP terminal.
If “RMD.MSPE = 1” is set, immediate stops or deceleration stops are performed when “STP = ON”.
Deceleration stop is for high-speed patterns only and immediate stop is for constant-speed patterns.

Multiple PCD2112As can be used for multiple axis control.
Connect the STP terminals of all LSIs and input the same STP signal.
This allows you to stop multiple axes of “RMD.MSPE = 1” simultaneously.

An interrupt is generated when an operation stops by STP signal input turning ON.
The interrupt factor can be checked by RIST.ISTP bit.

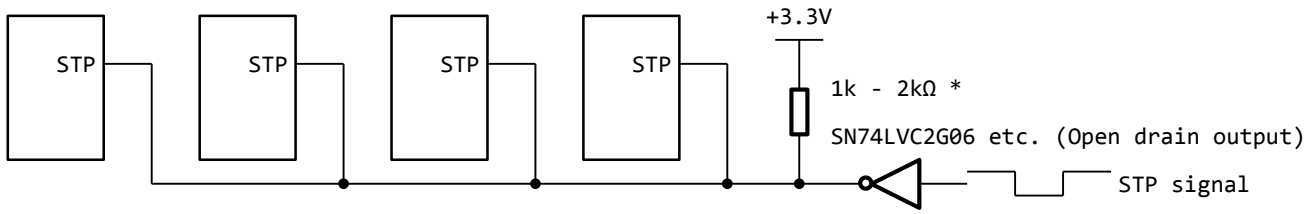
STP signal logic can be changed by RENV1.STPL bit.
The state of STP terminal can be monitored by RSTS.SSTP bit.

If “STP = ON”, the operation does not start with start command writing.

Even though the STP terminals of multiple LSIs are connected to each other, an axis can be stopped individually by stop command.

< External stop >

1) For simultaneous stop from an external circuit, connect as follows:




* STP terminal contains a pull-down resistor with a minimum of 40 kΩ.

2) Set “RMD.MSPE = 1” to the axes to be externally stopped, and start the operation.
3) Input one-shot signal from outside.
   Drive external STP signals with open drain outputs (SN74LVC2G06, etc.) before inputting.

Input one-shot signal of 0.5 µs or wider of STP signal when “RENV2.STAF = 0” is set.
Input one-shot signal of 40 ms or wider of STP signal when “RENV2.STAF = 1” is set.

| | |
|---|---|
| Waiting for STP signal input<br>0: Disabled.<br>1: Enabled. Immediate stop or deceleration stop will be performed. | RMD.MSPE(11) |
| Stop method by STP signal<br>0: Immediately stops.<br>1: Decelerates and stops. Immediately stops when operation is in constant-speed patterns. | RENV1.STPM(8) |
| STP signal logic<br>0: Negative logic.<br>1: Positive logic. | RENV1.STPL(9) |
| Input noise filter of STP terminal<br>0: Recognize signals with a pulse width of 0.5 µs or wider.<br>1: Recognize signals with a pulse width of 40 ms or wider. | RENV2.STAF(15) |
| STP terminal state<br>0: OFF.<br>1: ON. | RSTS.SSTP(30) |
| Interrupt by STP signal<br>0: Occurred.<br>1: Not occurred. | RIST.ISTP(2) |

# 10.9 Counter

## 10.9.1 Counter types and input methods

PCD2112A has RCUN register (remaining pulse number counter), and it has one RDWC register (current position counter) in addition.
RDWC register reads and obtains out RMV register values when operation mode starts, and counts down at every pulse output.

RCUN register has the following functions:

| Item | RCUN register specifications |
|---|---|
| Counter function | Up/down counter |
| Bit length | 32 bits including the sign (−2,147,483,648 to +2,147,483,647) |
| Counting input | Output pulses or encoder signal (EA and EB signals) inputs |

Encoder signals at the input of the counter can be selected from two input types by using RENV2.EIM bit.
1) Input 90-degree phase difference signal (multiplied by 1, 2, or 4)
   Count up when the phase of EA signal input is ahead of EB signal input; Count down when it is behind.
2) Input 2 pulses; up-pulse and down-pulse.
   Count up at the rising edge of EA signal input and count down at the rising edge of EB signal input.

| | |
|---|---|
| RCUN register input selection<br>0: Output pulse<br>1: Encoder signal (EA signal and EB signal) input | RENV2.CUNI(2) |
| EA and EB signal inputs<br>00: 90-degree phase difference; 1x 10: 90-degree phase difference; 4x<br>01: 90-degree phase difference; 2x 11: 2-pulse input; up and down | RENV2.EIM(9, 8) |
| Filters for EA, EB, and EZ signals<br>0: Recognize signals with a pulse width of 0.1 µs or wider.<br>1: Recognize signals with a pulse width of 0.3 µs or wider. | RENV2.EINF(10) |
| Interrupt by EA and EB signals<br>0: Disabled.<br>1: Enabled.<br>Input error occurs when;<br>- EA and EB signals change simultaneously during 90-degree phase difference mode.<br>- EA and EB signals rise simultaneously during 2-pulse mode. | RENV2.EECE(21) |
| Reading interrupt by EA and EB signals<br>0: Interrupt does not occur.<br>1: Interrupt occurred. | RIST.IECE(5) |
| Input of EA and EB signals<br>0: Disabled.<br>1: Enabled. | RENV2.EOFF(11) |
| Operation of RCUN register<br>0: Enabled.<br>1: Disabled. RCUN counting operation stops regardless of counter input. | RMD.MCCE(8) |

## 10.9.2 Clearing the counter to zero

CUNR (13h) command enables RCUN register (current position counter) cleared to zero.
When “RENV2.ORCR = 1” is set, the counter is cleared to zero when “origin return” is completed.

| | |
|---|---|
| RCUN counter is cleared to zero when origin return is completed<br>0: Disabled.<br>1: Enabled. | RENV2.ORCR(1) |
| Zero-clear command in RCUN register<br>RCUN register (current position counter) is cleared to zero. | CUNR(13h) |

# 10.10 ID monitor

ID code is built-in to distinguish PCD2112A from other LSI products.

The ID code can be checked by the following procedures:

1. Writes IDMON (03) command to the RCOM register.
2. Reads data at addresses “00” and “01”.

ID code can be read only when IDMON (03h) command is written to RCOM register.
When a command other than IDMON (03h) command is written, including NOP (00h) command, the ID code is shown by “0”.
The following table shows the ID codes of our products:

| LSI | ID code |
|---|---|
| PCD2112 | 0000h |
| PCD2112A | 0410h |

| | |
|---|---|
| ID Coding<br>Using IDMON (03h) command sets the ID code. | Address: 00h, 01h |
| ID code confirmation command<br>ID code is set to the addresses “00” and “01”. | IDMON(03h) |

# 11. Supplementary description of stand-alone operation system

## 11.1 EEPROM selection criteria

When PCD2112A is operated in a stand-alone operation, register values are automatically set from an externally connected 4-wire serial EEPROM.

**Table 11-1 EEPROM Selection Criteria**

<table>
<tr><th>Item</th><th>Content</th></tr>
<tr><td>Access method</td><td>SPI mode 0 is supported.</td></tr>
<tr><td>Capacity</td><td>16k bit or more (2k byte or more).</td></tr>
<tr><td>Maximum serial clock frequency</td><td>Equal to or more than the half of reference clock frequency.</td></tr>
<tr><td>Addressing</td><td>Specify the address in 16-bit.</td></tr>
<tr><td>Data size</td><td>8-bit unit.</td></tr>
<tr><td>Command</td><td>The following commands are valid.
<table>
<tr><th>Symbol</th><th>Instruction format</th><th>Content</th></tr>
<tr><td>WREN</td><td>0000 0110</td><td>Shift to writable mode</td></tr>
<tr><td>WRDI</td><td>0000 0100</td><td>Shift to write-prohibited mode</td></tr>
<tr><td>READ</td><td>0000 0011</td><td>Read command</td></tr>
</table></td></tr>
</table>

Note: I/F between PCD2112A and EEPROM can be established with the power supply of either 3.3 V or 5 V.
I/F between CPU and EEPROM may not be established if the power supply voltages of CPU and EEPROM are not equal.

Examples of EEPROM adoption: BR25H160F-2LB (ROHM), AT25160B (Microchip Technology), M95160 (STMicroelectronics), CAT15016 (ON Semiconductor).

# 11.2 Set the data to EEPROM

## 11.2.1 Set-up procedure

Set the data from CPU to EEPROM with the connection diagram in “2.5.2 Stand-alone operation system (MODE = H)”.
For EEPROM control procedures, see “5.6 Transition to EEPROM access mode”.

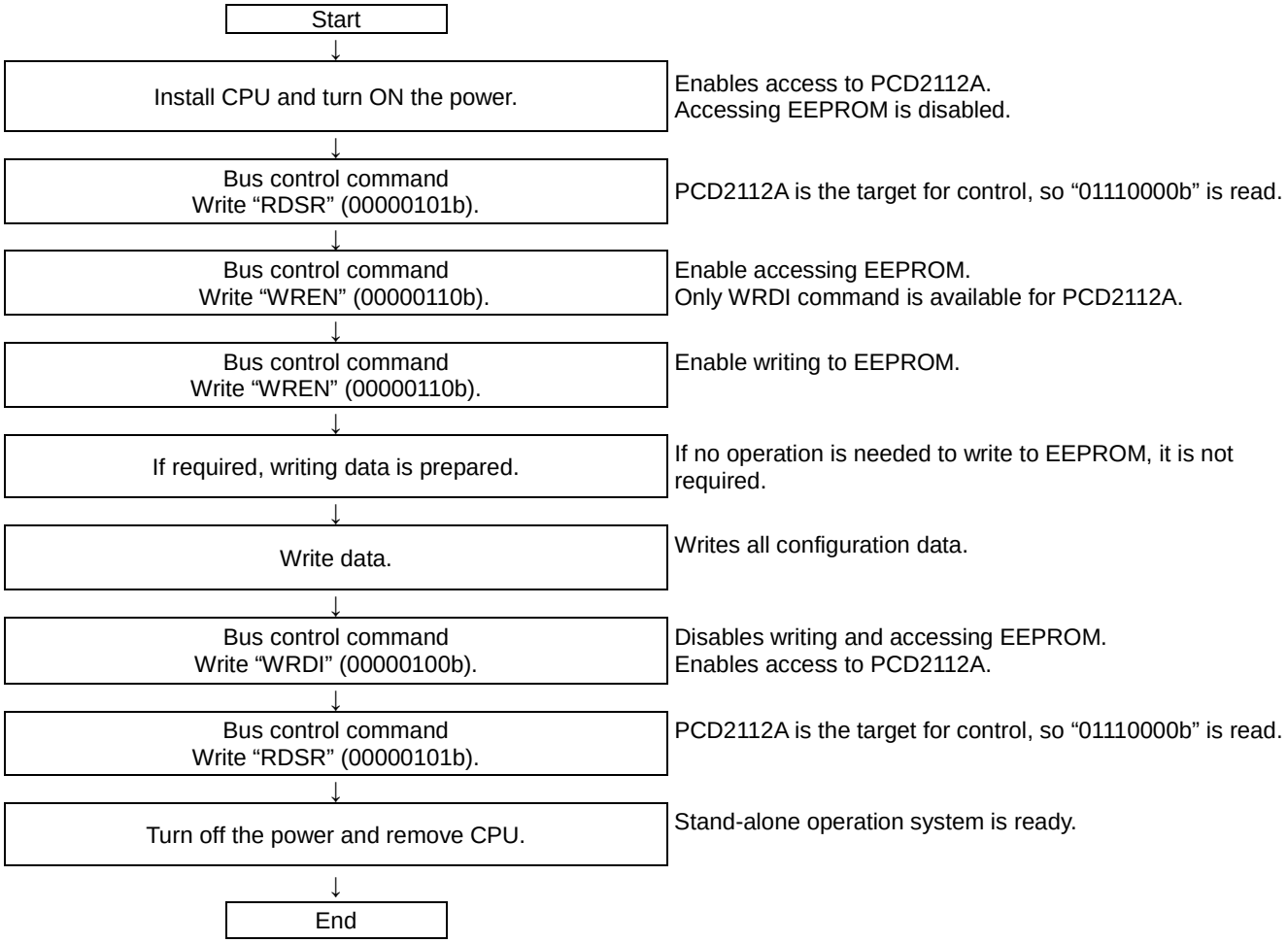



**Fig. 11.2-1 EEPROM Setting Procedures**

## 11.2.2 EEPROM address map

Up to 32 patterns of register values can be stored in EEPROM. (Pattern 0 to 31)
Each pattern is stored in the areas separated by every 64 byte.

| Address | EEPROM |
|---|---|
| 0000h | Pattern 0 |
| 0040h | Pattern 1 |
| 0080h | Pattern 2 |
| : | : |
| : | : |
| : | : |
| 0780h | Pattern 30 |
| 07C0h | Pattern 31 |
| 0800h | 0000 0000 |
| : | : |

| | Address | Offset |
|---|---|---|
| RENV2(31~24) | 0000h | 00h |
| RENV2(23~16) | 0001h | 01h |
| RENV2(15~ 8) | 0002h | 02h |
| RENV2(7~ 0) | 0003h | 03h |
| RENV1(31~24) | 0004h | 04h |
| : | : | : |
| : | : | : |
| RMD(15~ 8) | 001Fh | 1Fh |
| RMD(7~ 0) | 0020h | 20h |
| RCOM(7~ 0) | 0021h | 21h |
| 0000 0000 | 0022h | 22h |
| : | : | : |
| : | : | : |
| 0000 0000 | 003Fh | 3Fh |
| RENV2(31~24) | 0040h | 00h |
| RENV2(23~16) | 0041h | 01h |
| : | : | : |
| : | : | : |
| 0000 0000 | 007Fh | 3Fh |
| RENV2(31~24) | 0080h | 00h |
| : | : | : |
| : | : | : |

Note: The sequence of register values is the same as "4.1 Detailed memory map", but the address is shifted by 4 bytes.
Set the section from RENV 2 register to RCOM register as one unit of operation patterns.
Please store “0” in unused area.

# 12. Electrical characteristics

## 12.1 Absolute maximum ratings

| Item | Symbol | Rating | Unit | Description |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | −0.3 to +4.0 | V | - |
| Input voltage | $V_I$ | −0.3 to +7.0 | V | - |
| Output voltage | $V_O$ | −0.3 to +7.0 | V | - |
| Output current | $I_{OUT}$ | ±30 | mA | - |
| Storage temperature | $T_{stg}$ | −65 to +150 | ºC | - |

## 12.2 Recommended operating conditions

| Item | Symbol | Rating | Unit | Description |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | +3.3 ± 0.3 | V | - |
| Input voltage | $V_I$ | −0.3 to +5.8 | V | - |
| Ambient temperature | $T_A$ | −40 to +85 | ºC | $T_j$= −40 to +125 ºC, $\theta_{j\text{-}a}$=43 ºC/W |

## 12.3 DC characteristics

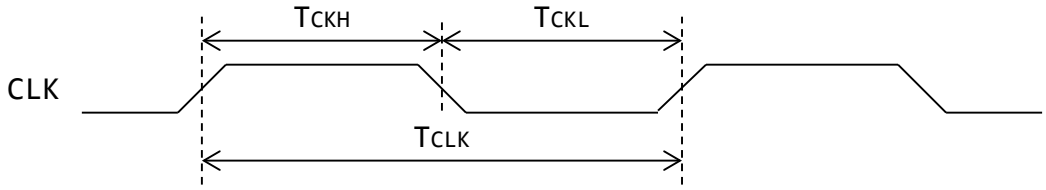
| Item | Symbol | Condition | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Current consumption | $I_{dd}$ | CLK = 9.8304 MHz, no load | | - | 9 | mA |
| | | CLK = 20.000 MHz, no load | | - | 19 | mA |
| Input capacitance | - | - | | - | 10 | pF |
| Low level input current | $I_{IL}$ | $V_{IH}$=$V_{DD}$, $V_{IL}$=GND | | −1 | +1 | µA |
| High level input current | $I_{IH}$ | $V_{IH}$=5.5 V | | - | 30 | µA |
| Low level input voltage | $V_{IL}$ | - | | −0.3 | 0.8 | V |
| High level input voltage | $V_{IH}$ | - | | 2.0 | 5.8 | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$=12 mA | *1 | - | 0.4 | V |
| | | $I_{OL}$=6 mA | *2 | - | 0.4 | |
| High level output voltage | $V_{OH}$ | $I_{OH}$=−12 mA | *1 | $V_{DD}$−0.4 | - | V |
| | | $I_{OH}$=−6 mA | *2 | $V_{DD}$−0.4 | - | |
| Low level output current | $I_{OL}$ | $V_{OL}$=0.4 V | *1 | - | 12 | mA |
| | | $V_{OL}$=0.4 V | *2 | - | 6 | |
| High level output current | $I_{OH}$ | $V_{OH}$=$V_{DD}$−0.4 V | *1 | −12 | - | mA |
| | | $V_{OH}$=$V_{DD}$−0.4 V | *2 | −6 | - | |
| Input rising time | Tr | - | | - | 50 | ns |
| Input falling time | Tf | - | | - | 50 | ns |
| Internal pull-down resistor | $R_{PD}$ | $V_I$ = $V_{DD}$ | | 40 | 240 | kΩ |

*1: ERC/CDW, BSY/END, OUT/PH1, DIR/PH2, P2/PH3, P3/PH4 terminals.
*2: Terminals other than the above.

# 12.4 AC characteristic

## 12.4.1 Reference clock

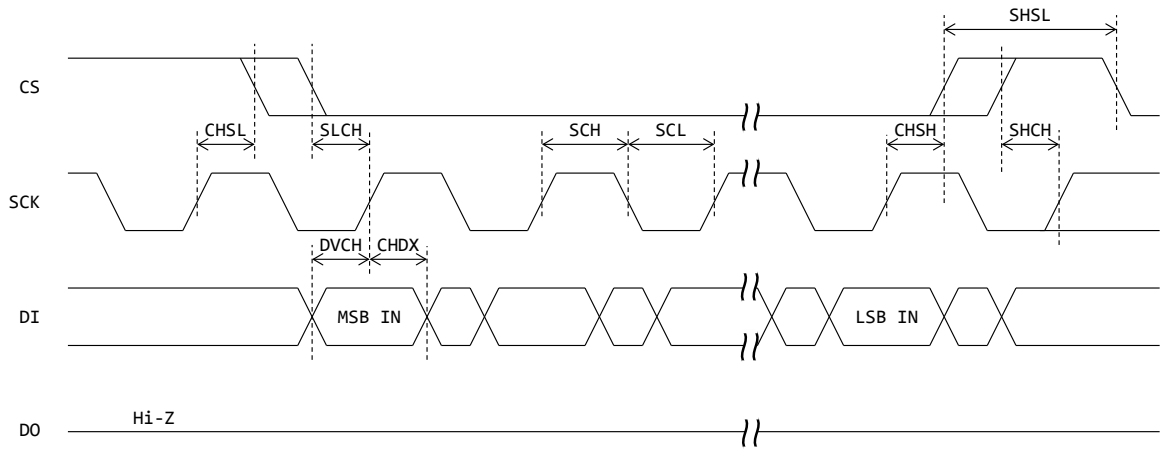
| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Reference clock frequency | $F_{CLK}$ | - | - | 20.5 | MHz |
| Reference clock cycle | $T_{CLK}$ | - | 48.8 | - | ns |
| Reference clock H level range | $T_{CKH}$ | - | 20 | - | ns |
| Reference clock L level range | $T_{CKL}$ | - | 20 | - | ns |



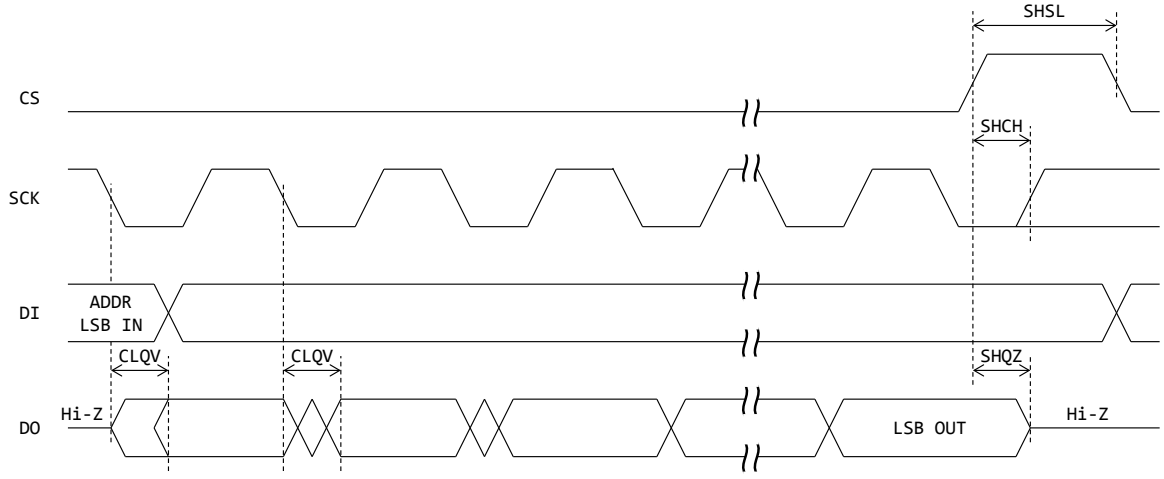
## 12.4.2 Serial bus I/F

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Serial clock frequency | $F_{SC}$ | - | - | $F_{CLK}$ | MHz |
| Serial clock cycle | $T_{SC}$ | - | $T_{CLK}$ | - | ns |
| Serial clock H time | SCH | - | 25 | - | ns |
| Serial clock L time | SCL | - | 18 | - | ns |
| CS active set-up | SLCH | - | 2 | - | ns |
| CS non-active set-up | SHCH | - | 0 | - | ns |
| CS de-select time | SHSL | - | $T_{SC}$ | - | ns |
| CS active hold time | CHSH | - | 1 | - | ns |
| CS non-active hold | CHSL | - | 0 | - | ns |
| Data set-up time | DVCH | - | 2 | - | ns |
| Data hold time | CHDX | - | 2 | - | ns |
| Output disable time | SHQZ | $C_L$ = 40 pF | - | 11+$T_{SC}$ | ns |
| Output delay time | CLQV | $C_L$ = 40 pF | - | 18 | ns |
| Delay of CSO falling edge | CSOF | $C_L$ = 40 pF | - | 12 | ns |
| Delay of CSO rising edge | CSOR | $C_L$ = 40 pF | - | 13 | ns |

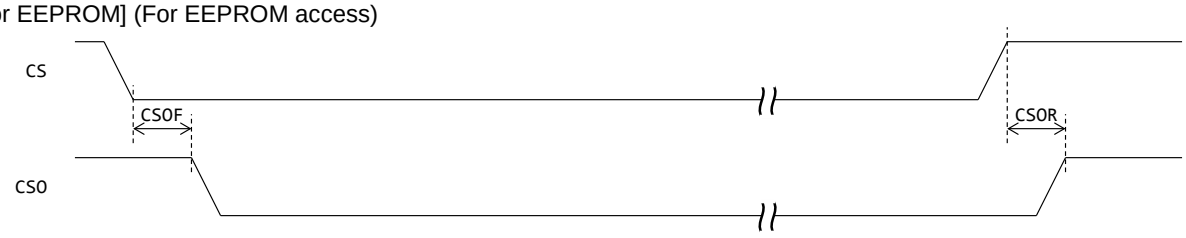
[Write timing]




[Read timing]



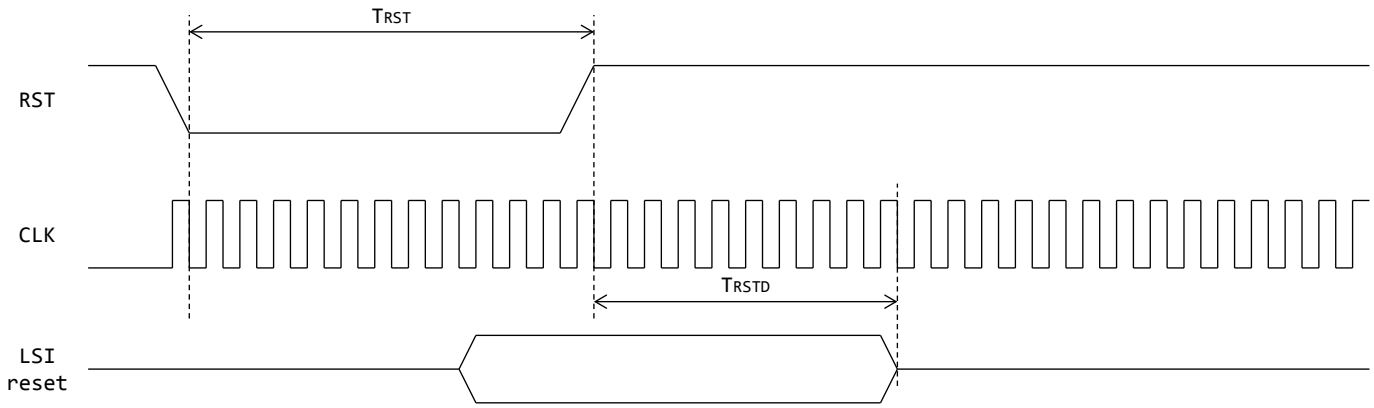

[CSO timing for EEPROM] (For EEPROM access)



# 12.5 Operation timings

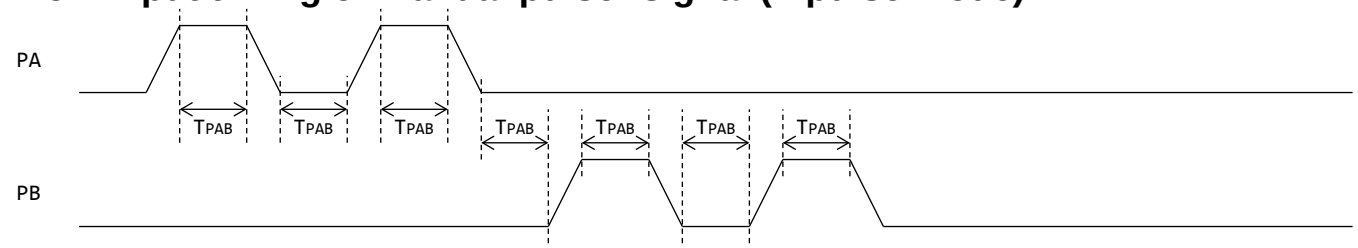
| Item | Abbreviation | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| RST input signal width | $T_{RST}$ | - | 8 | - | ×$T_{CLK}$ ns |
| Reset processing delay time | $T_{RSTD}$ | - | 8 | 9 | ×$T_{CLK}$ ns |
| PA and PB input signal width | $T_{PAB}$ | RENV2.PINF=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV2.PINF=1 | 3 | - | |
| PDR, MDR input signal width | $T_{DR}$ | RENV2.PINF=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV2.PINF=1 | 393,216 | - | |
| EA, EB, EZ input signal width | $T_{EAB}$ | RENV2.EINF=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV2.EINF=1 | 3 | - | |
| ORG input signal width | $T_{ORG}$ | RENV1.FLTR=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV1.FLTR=1 | 40 | - | |
| SD input signal width | $T_{SD}$ | RENV1.FLTR=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV1.FLTR=1 | 40 | - | |
| PEL, MEL input signal width | $T_{EL}$ | RENV1.FLTR=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV1.FLTR=1 | 40 | - | |
| STP input signal width | $T_{STP}$ | RENV2.STAF=0 | 5 | - | ×$T_{CLK}$ ns |
| | | RENV2.STAF=1 | 393,218 | - | |
| STA input signal width | $T_{STA}$ | RENV2.STAF=0 | 5 | - | ×$T_{CLK}$ ns |
| | | RENV2.STAF=1 | 393,218 | - | |
| STA output signal width | $T_{STO}$ | - | 8 | | ×$T_{CLK}$ ns |
| INP input signal width | $T_{INP}$ | RENV1.FLTR=0 | 1 | - | ×$T_{CLK}$ ns |
| | | RENV1.FLTR=1 | 40 | - | |
| ERC output signal width | - | RENV1.EPW= 000 | 125 | 126 | ×$T_{CLK}$ ns |
| | | RENV1.EPW= 001 | 992 | 1,008 | |
| | | RENV1.EPW= 010 | 3,968 | 4,032 | |
| | | RENV1.EPW= 011 | 15,872 | 16,128 | |
| | | RENV1.EPW= 100 | 126,976 | 129,024 | |
| | | RENV1.EPW= 101 | 507,904 | 516,096 | |
| | | RENV1.EPW= 110 | 1,015,808 | 1,032,192 | |
| ERC signal OFF timer time | - | RENV1.ETW= 001 | 125 | 126 | ×$T_{CLK}$ ns |
| | | RENV1.ETW= 010 | 15,872 | 16,128 | |
| | | RENV1.ETW= 011 | 507,904 | 516,096 | |
| | | RENV1.ETW= 100 | 1,015,808 | 1,032,192 | |
| | | RENV1.ETW= 101 | 2,031,616 | 2,064,384 | |
| | | RENV1.ETW= 110 | 4,063,232 | 4,128,768 | |
| | | RENV1.ETW= 111 | 8,126,464 | 8,257,536 | |
| BSY output ON delay time | $T_{BSYF1}$ | Command start | 5 | 6 | ×$T_{CLK}$ ns |
| | $T_{BSYF2}$ | STA signal start | 7 | 8 | |
| BSY output OFF delay time | $T_{BSYR}$ | - | 2 | | ×$T_{CLK}$ ns |
| Start delay time | $T_{OUTF}$ | - | 12 | | ×$T_{CLK}$ ns |
| Stand-alone operation SCK cycle | $T_{MC}$ | - | 2 | | ×$T_{CLK}$ ns |
| Stand-alone operation CSO delay time | $T_{MCSO}$ | - | 6 | 7 | ×$T_{CLK}$ ns |
| Stand-alone download time | $T_{MDLD}$ | - | 594 | | ×$T_{CLK}$ ns |

## 12.5.1 Reset signal input timing

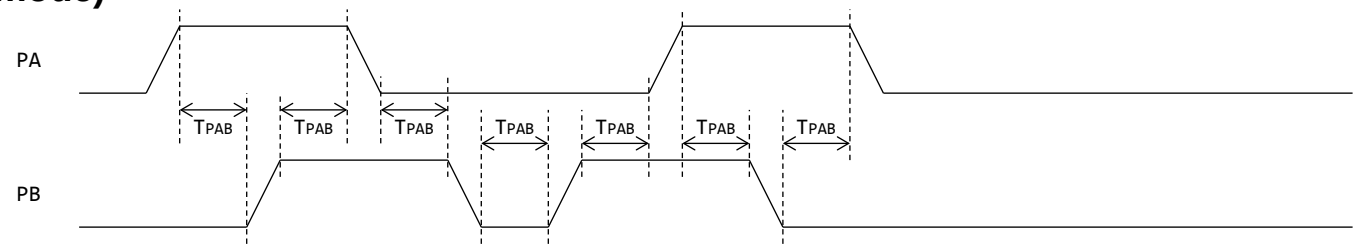



Note: Input CLK signal 8 times or more during “RST = L level”.
Thereafter, PCD2112A can be used after inputting CLK signals eight times or wider during “RST = H level”.

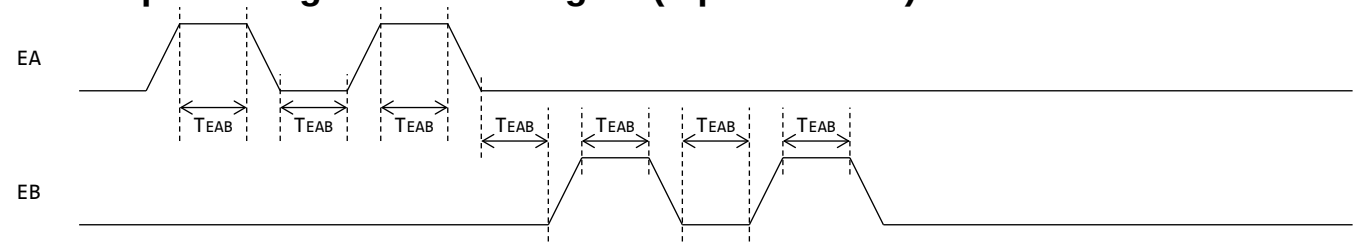
## 12.5.2 Input timing of manual pulser signal (2-pulse mode)



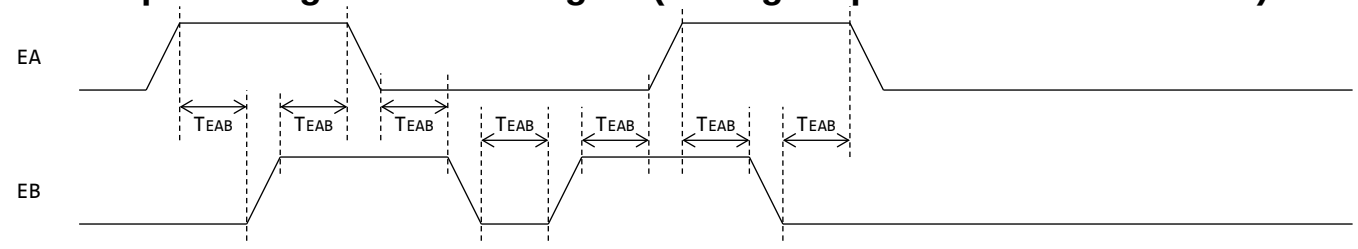

## 12.5.3 Input timing of manual pulser signal (90-degree phase difference mode)



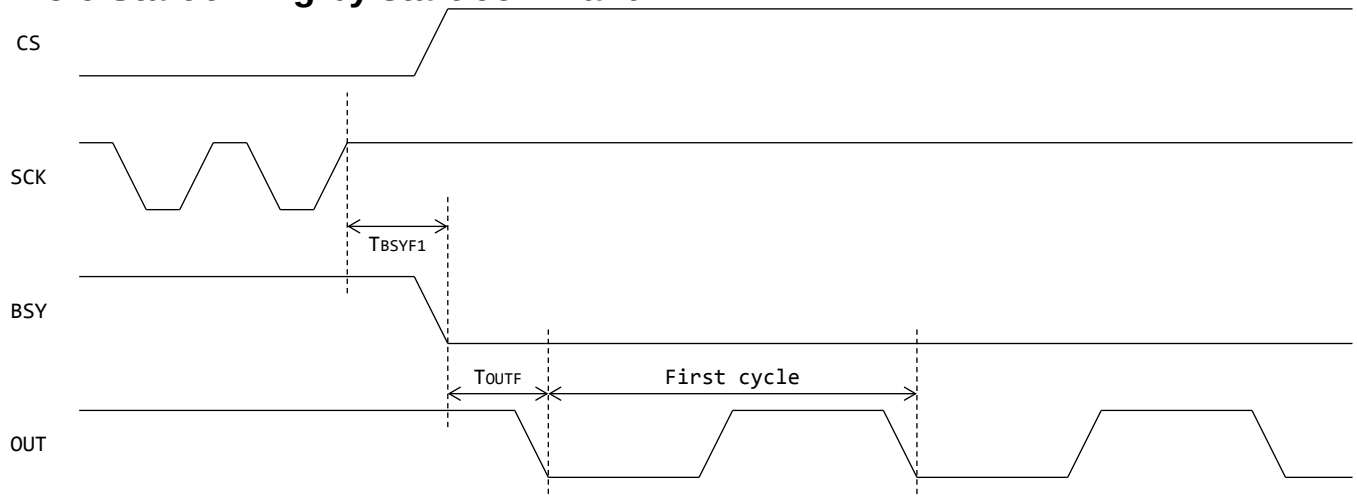

## 12.5.4 Input timing of encoder signal (2-pulse mode)



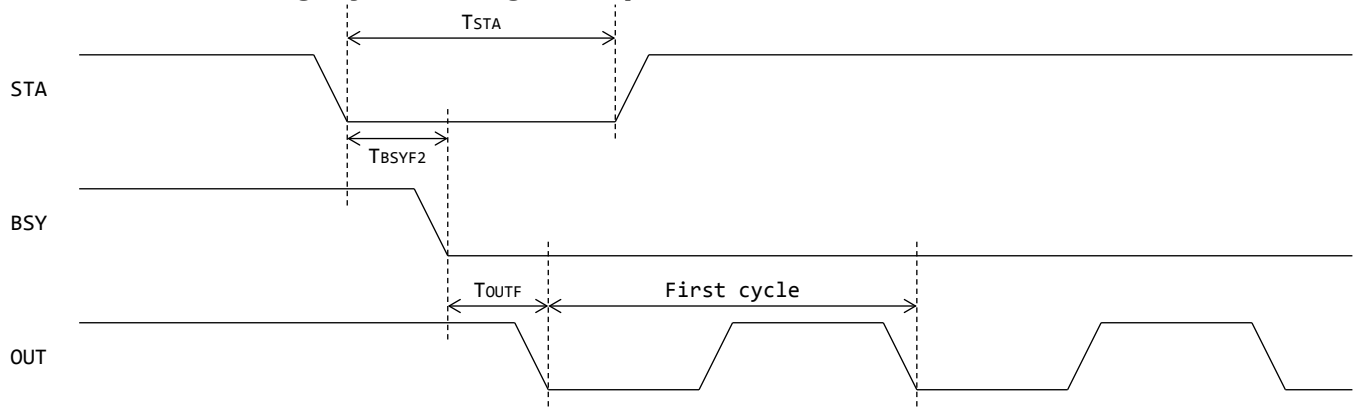

## 12.5.5 Input timing of encoder signal (90-degree phase difference mode)



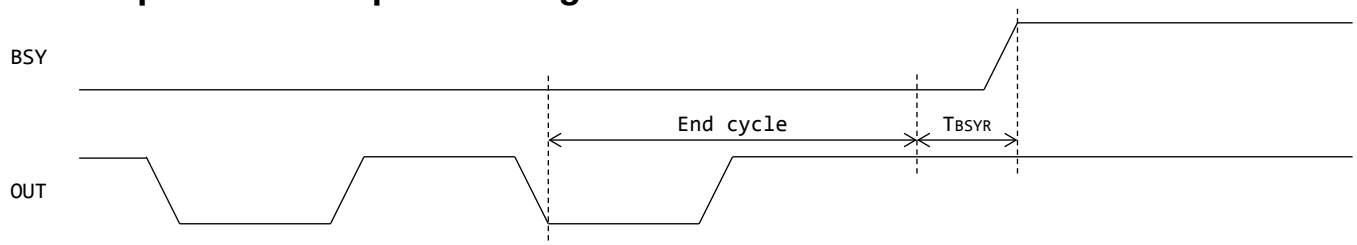
## 12.5.6 Start timing by start command



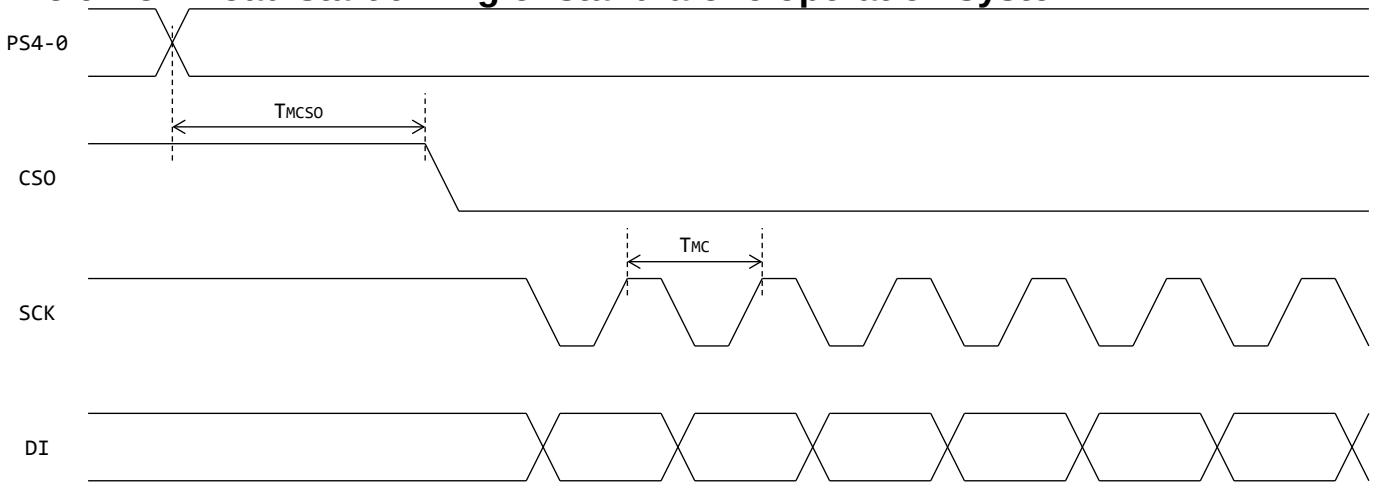

## 12.5.7 Start timing by start signal input



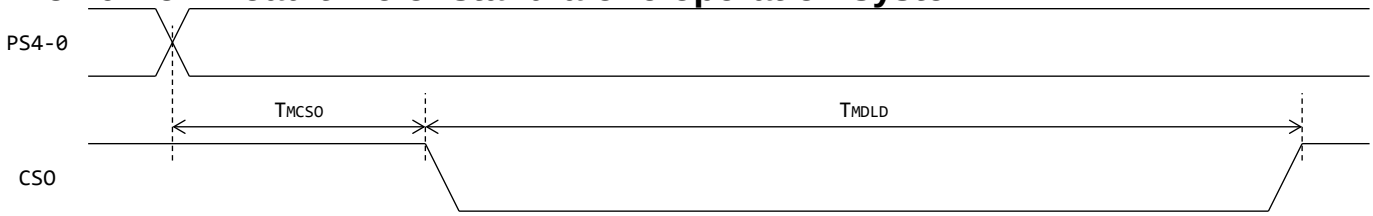

## 12.5.8 Operation complete timing



## 12.5.9 Download start timing of stand-alone operation system

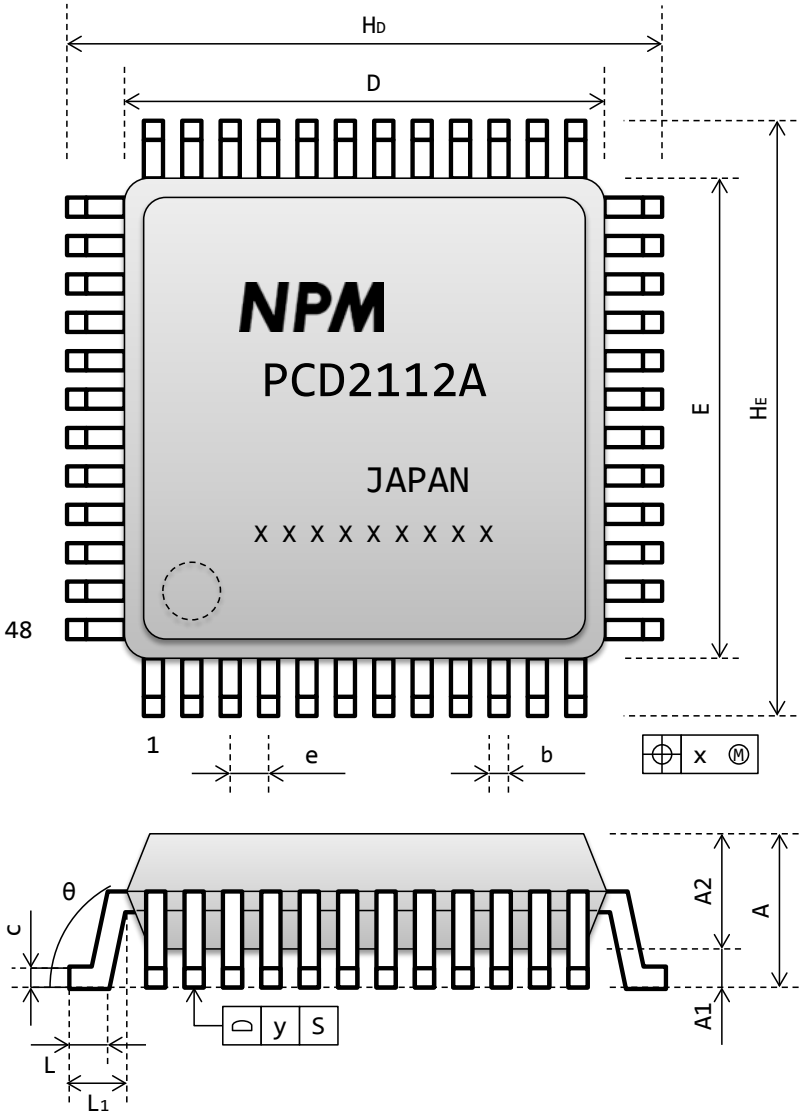



## 12.5.10 Download time of stand-alone operation system



# 13. External dimensions

(Plastic TQFP-48 pin)




| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Norm. | Max. |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| A | - | - | 1.20 |
| A1 | 0.00 | 0.10 | 0.20 |
| A2 | 0.90 | 1.00 | 1.10 |
| e | - | 0.50 | - |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | 0.15 | 0.20 |
| θ | 0° | 5° | 10° |
| L | 0.30 | 0.50 | 0.70 |
| $L_1$ | 0.80 | 1.00 | 1.20 |
| $H_D$ | 8.60 | 9.00 | 9.40 |
| $H_E$ | 8.60 | 9.00 | 9.40 |
| x | - | - | 0.08 |
| y | - | - | 0.10 |

# 14. Handling precautions

## 14.1 Design Precautions

1. Regarding operating voltage, current, temperature, input/output voltage / current etc., please use this product within the rated range.
   If used outside the rated range, even if it operates normally in the short-term, there is a possibility of increasing the failure rate.
   Even within the rated range, the failure rate varies depending on the operating temperature and voltage, so please consider this point when designing the equipment.
   Furthermore, please do not exceed the absolute maximum ratings even for a very short time.
2. Take precautions against the influence of heat in the environment, and keep the temperature around the LSI as cool as possible.
3. When latch-up phenomenon occurs, there is a danger of overheating and smoking. Pay attention to the following points.
   - Make sure that the voltage on the I/O terminals does not exceed the maximum ratings.
   - Consider power voltage drop timing when turning ON the power.
   - Be careful not to introduce external noise into the LSI.
   - Fix the potential of unused input terminals to $+V_{DD}$ or GND level, or pull-up or pull-down.
   - Pull-up or pull-down the potential of the unused bi-directional terminals.
   - Do not short-circuit the outputs.
   - This LSI should be protected from induction in high voltage generation circuit, static electricity, etc.
4. Do not apply overvoltage due to noise, surge voltage, static electricity, etc. to the LSI.

## 14.2 Precautions for Transportation and Storage

1. Handle LSIs and their packages carefully. Please do not throw or drop it. The LSI may be damaged or the aluminum laminate packaging material may be damaged and the airtightness may be impaired.
2. Do not store LSIs in a location exposed to water droplets or direct sunlight.
3. Do not store the LSI in a location where corrosive gases are present, or in excessively dusty environments.
4. Store the LSIs in an anti-static storage container, and make sure that no physical load is placed on the LSIs.
5. When transporting, follow the cautions on the packaging box.
6. The storage temperature should be 30°C or less and humidity should be 70% RH or less.
7. Keep LSIs in a place with little temperature change. Drastic temperature change during storage leads to dew condensation, lead frame oxidation, corrosion, etc., and causes bad solder wettability.
8. Place an antistatic mat on the storage shelf surface and ground the mat's surface.
   (Surface-earth resistance between $7.5 \times 10^5$ and $1 \times 10^9$ Ω)
9. When removing the LSI from packaging and storing it again, please use the antistatic storage container.

# 14.3 Precautions for Handling Environment

1. The humidity should be 40 to 70% considering moisture absorption after opening moisture-proof packaging products.
2. Make sure to ground all equipment, tools, and jigs that are present at the work site.
3. Ground the work floor using a conductive mat or similar apparatus (with an appropriate resistance factor) (Surface-earth resistance should be $1 \times 10^9$ Ω or less)
4. Ground the work desk surface using a conductive mat (Surface-earth resistance should be $7.5 \times 10^5$ to $1 \times 10^9$ Ω or less)
5. Do not cover the work surface with metal. Metal surface may cause abrupt discharge (if a charged LSI touches the surface directly) due to extremely low resistance.
6. When vacuum-sucking the surface of the LSI, take measures such as using a conductive rubber at the tip to prevent static electricity.
7. Do not touch LSI with electrified body (such as working wear, human body, etc.).
8. The surface of the display (such as cathode ray tube etc.) in the work area should be shielded from static electricity by OA equipment filter etc. Avoid turning ON/OFF during operation as much as possible.
9. Please use a conductive cover, conductive caster, etc. on the work chair and ground it to the floor.(Seat surface - ground resistance should be $1x\ 10^{10}$ Ω or less)
10. Workers should wear a wrist strap and ground it through a resistor.
    (When worn, the resistance between the surface and earth should be $7.5 \times 10^5$ to $3.5 \times 10^7$ Ω)
11. Handle the LSI package and the LSI carefully so as not to subject them to mechanical vibrations and impact.

# 14.4 Precautions for mounting

1. Plastic packages absorb moisture easily. Even if they are stored indoors, they will absorb moisture as time passes. If you put LSI in a reflow oven leaving moisture absorbed, cracks may occur in the resin or adhesion between the resin and the frame may deteriorate. Storage period before moisture proof bag opening is one year.
2. If you are worried about moisture absorption, dry the packages thoroughly before reflowing the solder.
   Dry the packages for 20 to 36 hours at 125 ± 5 °C. Do not dry more than two times.
3. If 30 days passes after opening moisture proof bag, the LSI will need to be dried.
   When soldering by a complete heating method like infrared reflow, please work under the following conditions. Reflow can be done up to 2 times.
   - The temperature profile of an infrared reflow furnace must be within the range shown in the figure below. (The temperatures shown are for the temperature at the surface of the plastic package.)

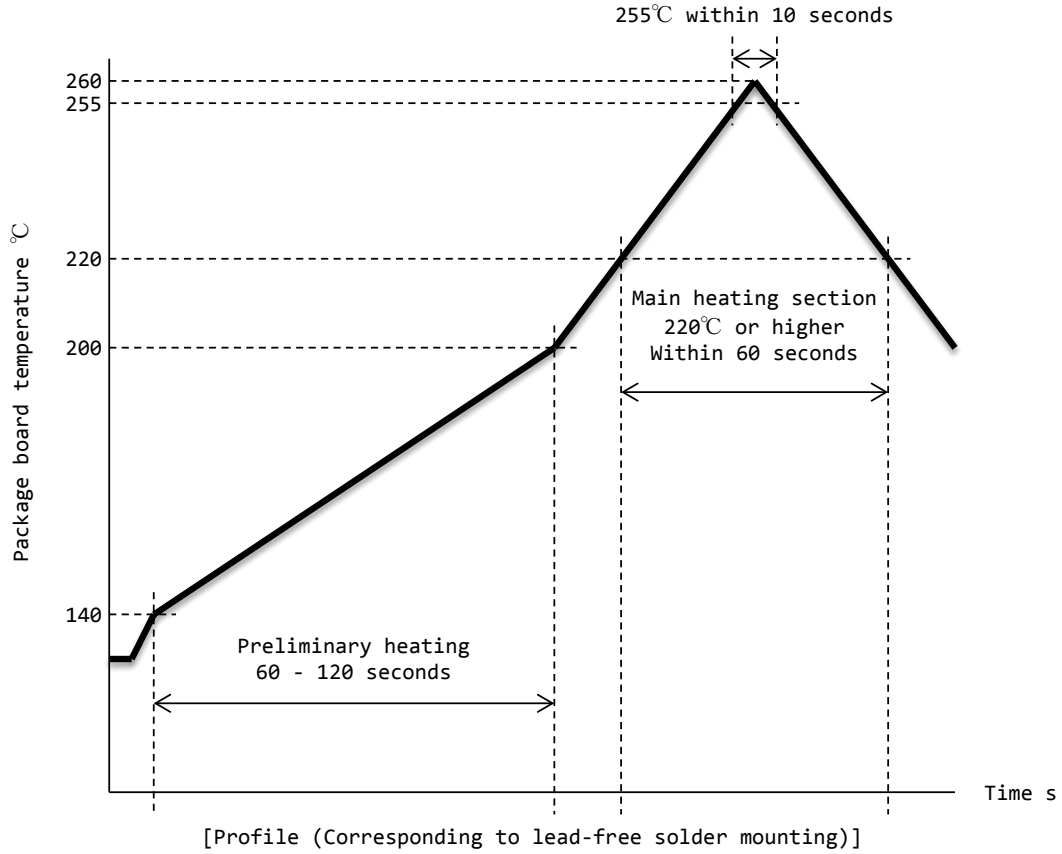



**Fig. 14.4-1 Profile (for lead-free solder mounting)**

4. Solder immersion method can cause rapid temperature change in the packages and may damage the LSI. Therefore, do not use this method.
5. Hand soldering work using a solder iron should be done under the following conditions.
   - Maximum temperature of the soldering iron 350 °C, maximum 5 seconds or less, 2 times or less.
   - Be careful that the solder iron does not touch parts other than the lead part, such as the package body.

# 15. Differences between PCD2112A and PCD2112

Some functions are added to PCD2112A based on conventional PCD2112; function improvements and defect corrections are implemented. If you use only the same functions as PCD2112, you can control them with PCD2112 software.
In this manual, errors and fluctuation of notation were corrected, omissions of description were added, and calculation formulas and values that are closer to actual circuits are adopted.

## 15.1 Additional functions

The following function was added to PCD2112A.

### 15.1.1 ID monitor

ID codes were added to distinguish between PCD2112 and PCD2112A.
See “10.10 ID monitor” for details.

## 15.2 Functional improvement

In PCD2112A, the following function is improved:

### 15.2.1 SCK signal input before control target LSI change

PCD2112 required the following procedures when connecting multiple LSIs.

1. Set to “CS=L level”.
2. Send SCK signal and DI signal to the current LSI to be controlled.
3. Set to “CS=H level”.
4. Input SCK signal one time or wider.
5. Set to “CS=L level”.
6. Send SCK signal and DI signal to the new LSI to be controlled.
7. Set to “CS=H level”.

PCD2112A does not require SCK signal to be input more than once.
Like the PCD2112, inputting SCK signal more than once does not cause any problems.

## 15.3 Correct non-conformity

In PCD2112A the followings items are corrected.

### 15.3.1 Writing emergency stop command during stopping

With PCD2112, the following procedures are required when an emergency stop command was used during stop.

1. Write EMGSP (30h) command when “RSTS.SCM = 0000b” (during stopping).
2. Write STOP (31h) command.
3. Start with STAFH1 (41h) command, etc.

With the PCD2112A, writing the STOP (31h) command is not needed.
Like PCD2112, writing the STOP (31h) commands does not cause any problems.

### 15.3.2 Slow-down point auto-setting by target speed override

In PCD2112, the following issues were occurred:

1. Slow-down point is set to “RMD.MSDP = 0” (auto).
2. Start incremental drive operation mode by positioning control, etc.
3. After the completion of acceleration, the target velocity is overridden, and the speed is re-accelerated.
4. Slow-down point auto-setting may not be able to follow re-acceleration.
   After deceleration, motor operates at FL speed or stops abruptly without decelerating to FL speed.

PCD2112A has been corrected so that slow-down point auto-setting can follow.
Though speed patterns differ from PCD2112, it does not affect the number of output pulses.

# 15.4 Package changes

PCD2112A and PCD2112 differ slightly in packaging because of differences in the manufacturing facilities.

## 15.4.1 Comparison of electrical characteristics

Differences in electrical characteristics are shown below.
For condition, see “12 Electrical characteristics”.

### 15.4.1.1 Comparison of absolute maximum ratings

| Item | Symbol | PCD2112 | PCD2112A | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | −0.5 to +4.6 | −0.3 to +4.0 | V |
| Input voltage | $V_I$ | −0.5 to +6.6 | −0.3 to +7.0 | V |
| Output voltage | $V_O$ | −0.5 to +6.6 | −0.3 to +7.0 | V |
| Output current (= 6 mA) *1 | $I_{OL}$ | 20 | ±30 | mA |
| Output current (> 6 mA) *2 | $I_{OH}$ | 30 | ±30 | mA |
| Storage temperature | $T_{stg}$ | −65 to +150 | | ºC |

*1: Other than the following terminals.
*2: ERC/CDW, BSY/END, OUT/PH1, P2/PH3, P3/PH4 terminals.

### 15.4.1.2 Comparison of recommended operating conditions

| Item | Symbol | PCD2112 | PCD2112A | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | +3.3 ± 0.3 | | V |
| Input voltage | $V_I$ | $V_{DD}$ | −0.3 to +5.8 | V |
| Ambient temperature | $T_A$ | −40 to +85 | | ºC |

### 15.4.1.3 Comparison of DC characteristics

| Item | Symbol | PCD2112 Min. | PCD2112A Min. | PCD2112 Max. | PCD2112A Max. | Unit |
|---|---|---|---|---|---|---|
| Current consumption(9.8304 MHz) | $I_{dd}$ | - | | 16 | 9 | mA |
| Current consumption (20.0000 MHz) | | - | | 31 | 19 | mA |
| Input capacitance | - | - | | 9 | 10 | pF |
| Low-level input current | $I_{IL}$ | - | | ±1 | | µA |
| High-level input current | $I_{IH}$ | 28 | - | 190 | 30 | µA |
| Low-level input voltage | $V_{IL}$ | 0 | −0.3 | 0.8 | | V |
| High-level input voltage | $V_{IH}$ | 2.0 | | 5.5 | 5.8 | V |
| Low-level output voltages | $V_{OL}$ | - | | 0.1 | 0.4 | V |
| High-level output voltages | $V_{OH}$ | $V_{DD}$ - 0.2 | $V_{DD}$ − 0.4 | - | | V |
| Low-level output current *1 | $I_{OL}$ | - | | 9 | 12 | mA |
| Low-level output current *2 | | - | | 6 | | |
| High-level output current *1 | $I_{OH}$ | −3 | -12 | - | | mA |
| High-level output current *2 | | −3 | -6 | - | | |
| Input rising time | Tr | - | | 200 | 50 | ns |
| Input fall time | Tf | - | | 200 | 50 | ns |
| Internal pull-down resistor | $R_{PD}$ | 18.9 | 40 | 107.1 | 240 | KΩ |

*1: ERC/CDW, BSY/END, OUT/PH1, P2/PH3, P3/PH4 terminals.
*2: Other than the above terminals.

## 15.4.2 Comparison of external dimensions

Differences in external dimensions are shown below:
See “13 External dimensions” for details.

| Symbol | | PCD2112A | PCD2112A |
|---|---|---|---|
| D | Min. | 6.8 | 6.90 |
| | Norm. | 7.0 | |
| | Max. | 7.2 | 7.10 |
| E | Min. | 6. 8 | 6.90 |
| | Norm. | 7.0 | |
| | Max. | 7.2 | 7.10 |
| A | Min. | 1.0 | - |
| | Norm. | 1.1 | - |
| | Max. | 1.2 | |
| A1 | Min. | 0.05 | 0.00 |
| | Norm. | 0.10 | |
| | Max. | 0.15 | 0.20 |
| A2 | Min. | - | 0.90 |
| | Norm. | 1.0 | |
| | Max. | - | 1.10 |
| e | Min. | - | |
| | Norm. | 0.5 | |
| | Max. | - | |
| b | Min. | 0.18 | 0.17 |
| | Norm. | 0.22 | |
| | Max. | 0.27 | |
| c | Min. | 0.10 | 0.09 |
| | Norm. | 0.17 | 0.15 |
| | Max. | 0.20 | |
| θ | Min. | 0 | |
| | Norm. | 3 | 5 |
| | Max. | 7 | 10 |
| L | Min. | 0.45 | 0.30 |
| | Norm. | 0.60 | 0.50 |
| | Max. | 0.75 | 0.70 |
| $L_1$ | Min. | 0.8 | |
| | Norm. | 1.0 | |
| | Max. | 1.2 | |
| $H_D$ | Min. | 8.8 | 8.60 |
| | Norm. | 9.0 | |
| | Max. | 9.2 | 9.40 |
| $H_E$ | Min. | 8.8 | 8.60 |
| | Norm. | 9.0 | |
| | Max. | 9.2 | 9.40 |
| x | Min. | - | |
| | Norm. | - | |
| | Max. | 0.10 | 0.08 |
| y | Min. | - | |
| | Norm. | - | |
| | Max. | 0.08 | 0.10 |

(Dimension in Millimeters)

## 15.4.3 Comparison of precautions for mounting

Differences in mounting precautions are shown below:
See “14.4 Precautions for mounting”.

### 15.4.3.1 Storage conditions before mounting (before unsealed)

| Item | PCD2112 | PCD2112A |
|---|---|---|
| Relative humidity | - | 30ºC 85% RH or less |
| Period | For one year | |

### 15.4.3.2 Storage Conditions before mounting (after unsealed)

| Item | PCD2112 | PCD2112A |
|---|---|---|
| Relative humidity | - | 30ºC 70% RH or less |
| Period | 3 days | 30 days |

### 15.4.3.3 Recommended drying conditions

| Item | PCD2112 | PCD2112A |
|---|---|---|
| Temperature | 125ºC | 125 ± 5ºC |
| Time (Lower limit) | 10 times | 20 times |
| Time (Upper limit) | 72 times | 36 times |
| Number of times (Upper limit) | 1 time | 2 times |

### 15.4.3.4 Allowable temperature profile conditions

| Item | PCD2112 | PCD2112A |
|---|---|---|
| Maximum peak temperature | - | 260ºC |
| Main heating temperature (upper limit) | 260ºC | 255ºC |
| Main heating temperature (upper limit) time | 10 seconds | |
| Main heating temperature (lower limit) | 220ºC | |
| Main heating time (Upper limit) | 60 seconds | |
| Preheating temperature (upper limit) | 180ºC | 200ºC |
| Preheating temperature (lower limit) | 160ºC | 140ºC |
| Preheating time (Upper limit) | 120 seconds | |
| Preheating time (Lower limit) | 60 seconds | |
| Chlorine content * | Not more than 0.2% | - |
| Number of times (Upper limit) | 2 times | |

*: The chlorine content of the rosin-based flux (mass percentage).

### 15.4.3.5 Hand soldering conditions

| Item | PCD2112 | PCD2112A |
|---|---|---|
| Tip temperature (upper limit) | - | 350ºC |
| Time (Upper limit) | - | 5 seconds |
| Number of times (Upper limit) | - | 2 times |

## Revision

| Revision | Date | Contents |
|---|---|---|
| First | February 19, 2019 | New document. |

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